ANALYSIS AND MODELING OF STRESS RELATED EFFECTS IN SCALED SILICON TECHNOLOGY

By

SAMIR CHAUDHRY

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Abstract of Dissertation Presented to the Graduate School
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By

SAMIR CHAUDHRY

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Chairman: Dr. Mark E. Law
Major Department: Electrical and Computer Engineering

Based on the current understanding of stress related problems in silicon technology, the critical sources of stress in the silicon substrate are identified as ion-implanted dislocation loops, patterned and continuous thin films, and lattice mismatched epitaxial films.

The stress from dislocation loops is found to be a strong function of the dislocation loop ensemble properties. A model based on the Ostwald ripening phenomenon is developed to predict the evolution of dislocation loops in an inert ambient. Bounds for a critical radius, below which the dislocation loops dissolve and shrink, and above which they grow, are defined. The stress from a given ensemble of dislocation loops is modeled by calculating the extra number of atoms in the silicon substrate. This is used as an initial loading strain force in a finite element solver to predict the stress in the substrate. The peak value of the strain is experimentally verified using x-ray rocking curve analysis. The tensile component of the substrate stress at the loop layer edges is found to be strongly sensitive to the displacement boundary condition at the lateral edges of the simulation structure.

A numerical model, based on a balance of forces finite element solver, is developed to predict the stress in the silicon substrate from patterned and continuous films. The intrinsic or thermal mismatch stress is used as a initial loading condition on the structure. The wafer bow predicted by the model is in agreement with the experimentally extracted values.

The effect of stress from multiple nitride stripes on the diffusion of phosphorus and the evolution of dislocation loops is experimentally investigated. As compared to the tensed regions of the substrate, regions of compression show retarded diffusion of phosphorus, and a smaller size and density of the dislocation loops. A simulation scheme is developed to investigate the main mechanisms responsible for this anomalous behavior. Based on the results of the simulations, upper bounds for the elastic inclusion volumes of point defects and dopant-point defect pairs are extracted.

CHAPTER I
INTRODUCTION

The reduction in active device dimensions to micron and sub-micron geometries has resulted in an intimate coupling of process conditions, device behavior, and circuit performance to a degree unknown a few years ago. Due to the inherent complexity of integrated chip (IC) processing, it is becoming progressively more difficult to develop new processes. A modern IC process contains several hundred individual steps. The use of computer aided design tools has proven to be invaluable in new technology development and IC design. Computer simulations have also emerged as a very elegant way to aid process and device engineers in their task of finding an optimum process for a given device or circuit design.

The traditional "trial-and-error" experimental approach used to develop new technologies starts with an existing process. Together with structural dimensions, certain process steps are then altered to fabricate several lots. Completed test structures are subsequently evaluated to investigate if the original goals have been met. In Figure 1.1, route A schematically describes this approach, which might require several iterations to optimize the new process [1].

The application of software tools in the development of new processes and novel device structures has become a worthwhile, albeit challenging, alternative to the experimental route (see path B in Figure 1.1). Fabricating one lot in a modern process can cost upwards of 10,000 dollars, and consume weeks or even months of effort. The use of accurate simulation tools in the proper computing environment allows for comparatively inexpensive "computer experiments."

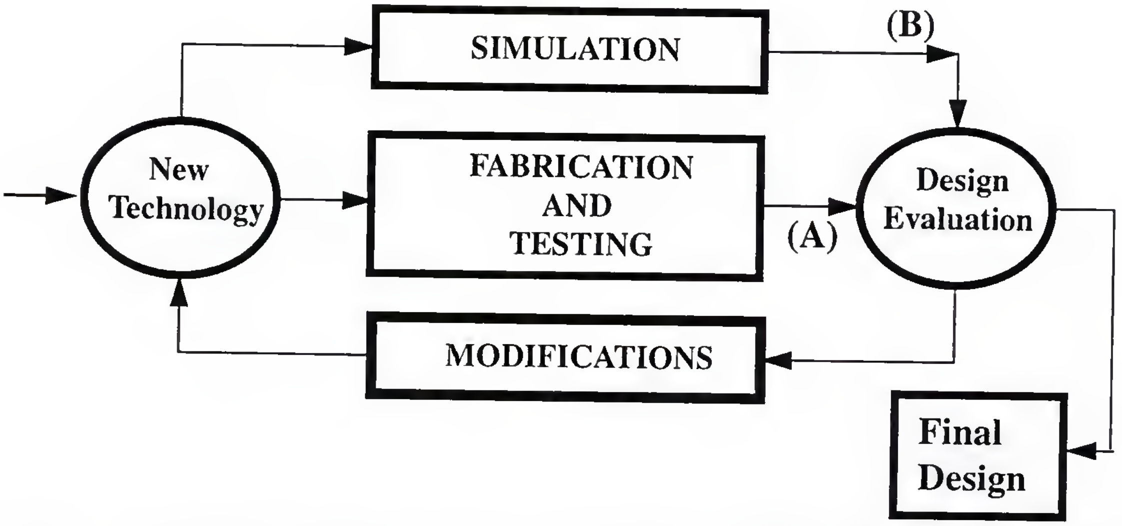


Figure 1.1 Simulation and experiment as alternative routes in development of new technologies. Route B would eventually involve a run through Route A, but helps in considerably lowering the time and expense of Route A.

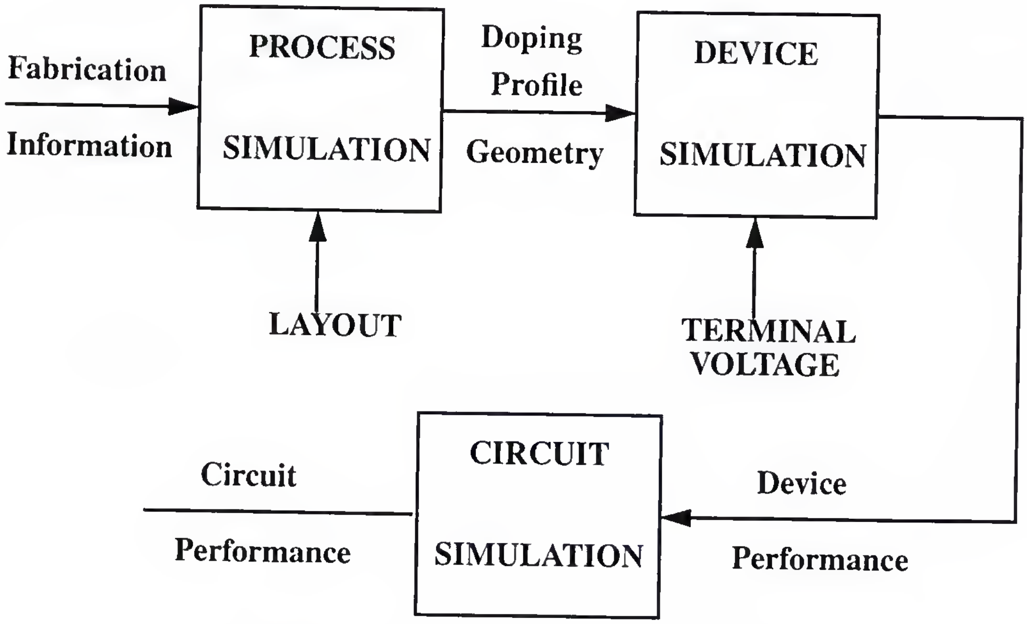


Figure 1.2 Process simulation as part of the general simulation methodology.

Figure 1.2 schematically illustrates the various software aids for IC technology development. Process simulation deals with all aspects of IC fabrication. With the proper input parameters (process recipes, layout geometries), process simulation determines the details of the resulting device structure, such as the boundaries of different materials and the distribution of impurity ions.

The complex fabrication technique used to make the modern day silicon IC involves the contiguous embedding, butting, and overlaying of structural elements. Such elements, with vastly different thermal and elastic properties, develop stress during the thermal cycling of the chip. Furthermore, many of the materials used in silicon technology such as CVD (Chemical Vapor Deposition) silicon nitride, silicon dioxide, polycrystalline silicon, etc., by virtue of their formation processes, exhibit intrinsic stresses. Large localized stresses are induced in the silicon substrate near the edges and corners of such structural elements. Oxidation of non-planar surfaces, frequently encountered in ULSI (Ultra Large Scale Integration) processing, produces another kind of stress in the substrate that can be very damaging, especially at low oxidation temperatures. Mismatch of atomic sizes between dopants and silicon atoms produces another kind of strain that can lead to the formation of misfit dislocations.

1.1 Stress and Strain

Before proceeding with a discussion on some of the stress related issues in silicon technology, this sections reviews the fundamental physics associated with studying material deformation.

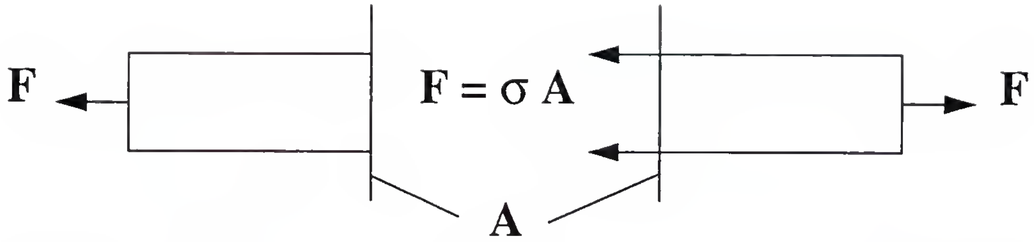


Figure 1.3 Figure illustrating the idea of stress: a body to which a stretching force is applied.

The basic idea of stress can be understood by considering a body (Figure 1.3) to which a stretching force F is applied. The force has a tendency to "stretch" the specimen, breaking the internal bonds. The bond-breaking is opposed by internal reactions in the body, called *stresses*.

The best way of visualizing these stresses is by the method of analysis used in mechanics of materials: the specimen is "sectioned" and the missing part is replaced by the forces that it was exerting (Figure 1.3). In this case the "resistance" is uniformly distributed over the normal section, as shown by the two arrows. The normal stress σ is defined as the "resistance" per unit area. Applying the equilibrium of forces principle to the right side portion of the specimen:

$$\begin{aligned} \sum F &= 0 \\ F - \sigma A &= 0 \qquad \text{1-1} \\ \sigma &= F/A \end{aligned}$$

This is the internal resisting stress opposing the externally applied load, thereby preventing the sample from fracturing. As the applied force F increases, so does the length of the specimen. For an increase of dF, the length l increases by dl. The normalized (per unit length) increase in length is equal to

$$d\varepsilon = dl/l \text{ or integrating } \varepsilon = \int_{l_0}^{l_1} dl/l = \ln\frac{l_1}{l_0} \qquad \text{1-2}$$

where l_0 and l_1 are the initial and final lengths of the specimen, respectively, and ε is the longitudinal strain.

Another frequent form of deformation commonly encountered in semiconductor engineering is the shear strain. To illustrate shear, consider a circular cylindrical shaft, as shown in Figure 1.4 (a). When the shaft is twisted, the elements in the shaft are distorted in the manner shown in Figure 1.4 (b). In this case the angle α may be taken as a measure of the strain. However, it is customary to treat tan α as the shear strain.

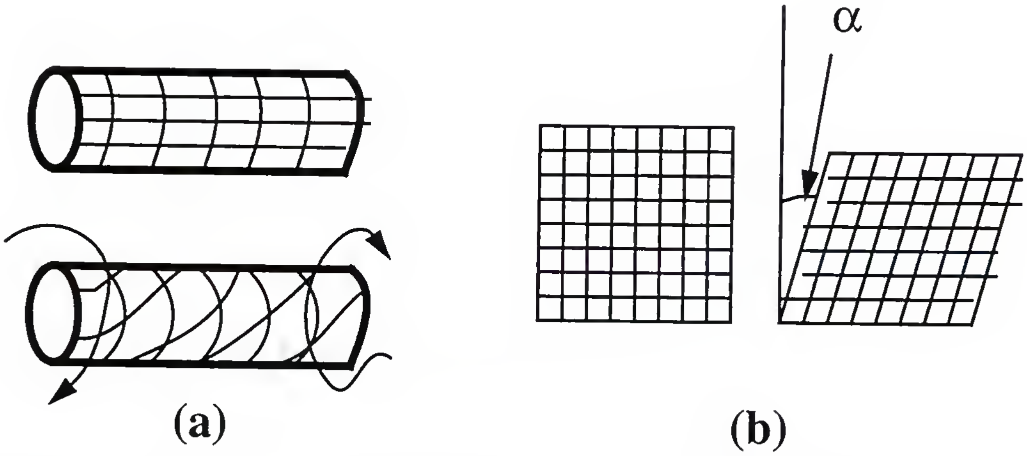


Figure 1.4 The shear pattern of deformation (a) twisting, and (b) simple shear.

The selection of proper measures of strain is dictated basically by the stress-strain relationship (i.e., the constitutive equation of the material). For example, if we pull a string, it elongates. The experimental results can be presented as a curve of the tensile stress σ plotted against the strain ε. An empirical formula relating σ to ε can then be determined. For most engineering materials subjected to infinitesimal strain in uniaxial stretching, a relation, like

$$\sigma = E\varepsilon \tag{1-3}$$

where E is a constant called *Young's modulus,* is valid within a certain range of stresses. Equation 1-3 is called *Hooke's law*, and a material obeying it is called a *Hookean material.* Corresponding to Equation 1-3, the relationship for a Hookean material subjected to an infinitesimal shear strain is

$$\tau = G \cdot \tan\alpha \tag{1-4}$$

where G is another constant called the shear modulus or modulus of rigidity. The range of validity of Equation 1-4 is again bound by a yield stress, this time in shear. The yield stresses in tension, compression, and in shear are generally different. Deformations of most materials in nature and in engineering are much more complex than those discussed. Therefore, general method of treatment is needed. However, the general mathematical description of deformation is described first.

Let a body occupy space S. Referred to a rectangular cartesian frame, every particle in the body has a set of coordinates. When the body is deformed, every particle takes up a new position, described by a new set of coordinates. For example, a particle P, located originally at a point (a_1, a_2, a_3), is moved to a point Q (x_1, x_2, x_3) when the body moves and deforms. The vector $\overrightarrow{PQ}$ (Figure 1.5) is called the displacement vector of the particle under consideration, and its components are

$$x_1 - a_1, x_2 - a_2, x_3 - a_3 \qquad \text{1-5}$$

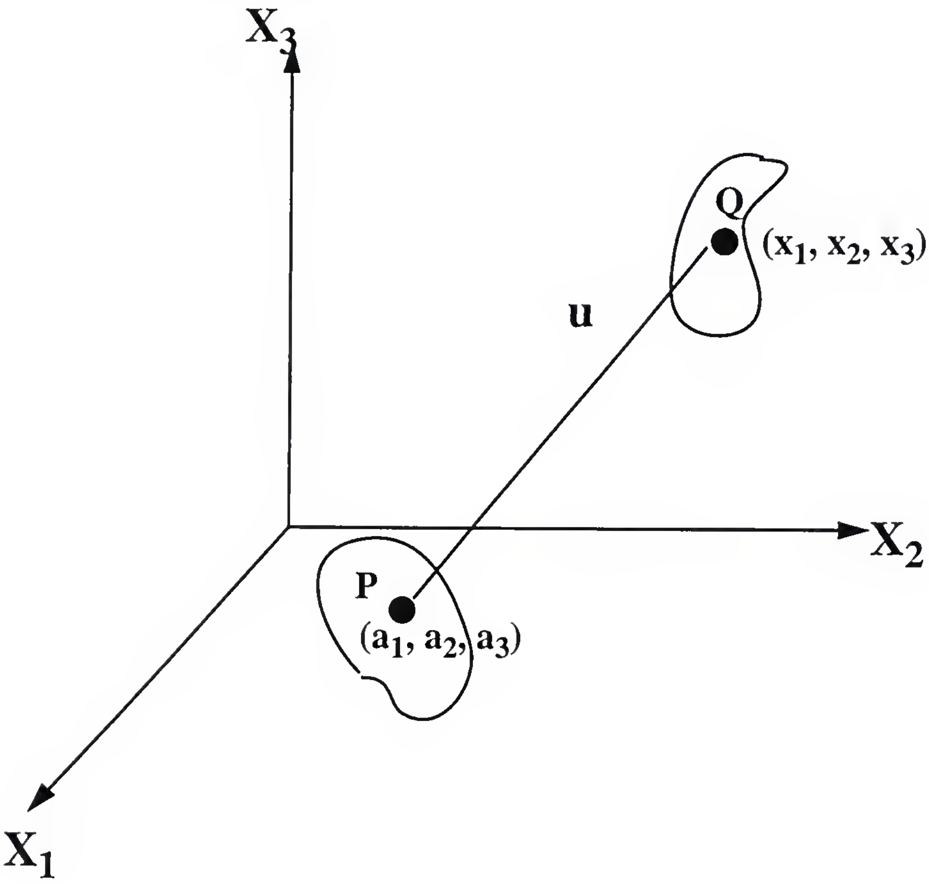


Figure 1.5 Displacement vector of a body that has been moved and deformed.

If the displacement is known for every particle in the body, the deformed body can be constructed from the original structure. Hence, the deformation can be described by a displacement field. Let the variable (a_1, a_2, a_3) refer to any particle in the original configuration of the body, and let (x_1, x_2, x_3) be the coordinates of that particle when the body is deformed. Then the deformation of the body is known if (x_1, x_2, x_3) are known functions of (a_1, a_2, a_3) :

$$x_i = x_i(a_1, a_2, a_3) \qquad 1\text{-}6$$

This is a transformation (mapping) from (a_1, a_2, a_3) to (x_1, x_2, x_3) . Subject to the assumptions of continuum mechanics, the displacement vector **u** is then defined by its components $u_i = x_i - a_i$.

1.2 Stress Related Issues in Silicon Technology

Stress related problems are pervasive and critical in ULSI technology. Many problems of defective devices in silicon integrated circuits can be ultimately traced to stresses that develop at various stages of I.C. processing. These problems grow more acute as I.C. devices become smaller in size and more complex in geometry and material mix. It is thus important to understand the nature and the origins of these problems. A clear understanding of these effects would aid engineers attempting to alleviate stress related problems in silicon technologies. In addition, quantitative modeling of these effects would be useful in designing processes and devices for optimal performance. The following sections attempt to bring out the origins of the aforementioned stress problems and their possible effects on device properties.

1.2.1 Stress from Thermal Processing

One class of stress problems, called thermal stress, arises from nonuniform temperature distribution within a silicon wafer. It remains an ever present problem in IC thermal processing, where transient temperature gradients are produced in silicon wafers during heating up and cooling down. The main symptoms of this problem were wafer warpage and slips and emerged when the size of the silicon wafer was increased from 1 to 2 inches. This problem was first recognized and analyzed in detail in 1969 by Hu [2] with the introduction of the concept of radiative heat transfer. In his model, an area element dA emits radiant energy at a rate that is proportional to the fourth power of its absolute temperature. The same area element also receives radiant energy from all area elements dA' in each of the two immediately neighboring wafers; these elements being at different temperatures over the entire wafer area A'. If the row of wafer is assumed to be infinitely long, then the temperature distribution in the two neighboring wafers is exactly the same as that in the subject wafer. The analysis reveals that the central region of the wafer cools down or heats up more slowly than the outer regions, setting up a radial temperature gradient, whose magnitude increases with the rate of heating or cooling. The maximum transient temperature difference between the center and edge of the wafer also increases with processing temperature and with the wafer diameter to spacing ratio. Various extensions to Hu's analyses have been made over the years [3,4].

At some stage during cooling, the thermal stress may exceed a threshold and is relieved via plastic deformation. At the final room temperature, the plastic strain introduced during cooling becomes frozen in, causing stress to be developed with a radial distribution which is approximately a reverse of that existing when the plastic deformation took place. Analyses [2,5] have shown the wafer will then warp with an anticlastic geometry; a universal saddle shape for <100> wafers.

1.2.2 Film Stress and Film Edge Induced Stress

Another class of stress problems arise when films such as silicon dioxide, silicon nitride, aluminum, or polycrystalline silicon are overlaid on silicon substrates [6]. Stress exists in these films both because of their thermal expansion mismatch and mechanistics of the film growth processes. Stress from the latter source is called "intrinsic stress." Continuous films produce only very low levels of stress in the substrate. This is because the substrate is usually about three orders of magnitude thicker than the surface films, and consequently, the stress level in the silicon substrate is lower than the film stress (as large as a few GPa) by three orders of magnitude. Problems occur when the surface films are not planar or contain certain discontinuities such as window edges. These discontinuities produce large localized stresses in the silicon substrates.

Direct dislocation generation at the edges of polycrystalline silicon stripes on silicon dioxide has been reported for charge coupled (CCD) devices [7]. Direct dislocation generation at the nitride edge has been observed [8] for film thicknesses larger than 200 nm deposited on bare silicon. These are usually 60° dislocations, and when the nitride edge is not in the <110> direction, form loops that straddle the edge. If there is a pad oxide layer between the silicon nitride film and the silicon substrate, no dislocation is directly generated when heat treated in a nitrogen ambient at temperatures as high as 1100°C [8].

Though a thicker pad oxide could be used to alleviate the harmful effects of stress in the substrate, it makes the nitride a less effective diffusion mask when used in an isolation scheme called local oxidation of silicon (LOCOS), and leads to a longer "bird's beak." The bird's beak which forms an unintended oxide wedge between the silicon nitride edge and the silicon substrate, stands in the way of device size reduction. The minimum thickness of the pad oxide required to prevent the formation of defective oxides has been studied by Bogh and Gaind [9] and Magdo and Bogh [10]. Much thinner pad oxide requirements have also been reported [11].

Dislocation generation due to nitride edges frequently occurs via indirect means. Thermal oxidation of silicon generates interstitials, some of which drift to the nitride edge and help nucleate dislocation loops there [12 - 14]. Bogh and Gaind [9] observed the formation of loops under nitride edges when the anneals were carried out in an oxidizing ambient. However, loops were absent in samples annealed in a nitrogen ambient for nitride thicknesses upto 166 nm.

In their study Hu and Schwenker [15] demonstrated the interaction of point defects with a nitride film edge. Point defects introduced in the substrate via ion-implantation formed dislocations which were clustered around the edge of the nitride stripe. Regions masked out from the ion-implantation showed no such dislocations. Another frequently observed process by which dislocation loops are generated at nitride edges was proposed by Hu et al. [16]. An inclined edge or 60° dislocation introduces an extra half lattice plane that extends either obliquely upward or downward. The dislocation is attracted to the nitride covered region if the extra half plane extends upward and is repulsed when the extra half plane extends downward. Figure 1.6 illustrates how a film edge induced stress field interacts with a moving dislocation. A dislocation, travelling to the right, introduces an oblique extra half plane that extends downward. It experiences repulsion at the nitride edge and starts to bend upward, inverting the sense of its associated half plane which is now obliquely upward. The right hand side dislocation half loop, in contrast to the left segment, now experiences a driving force to the right, so that the loop gets pulled out at both ends and cannot collapse despite the line tension. It then permanently straddles the film edge. The dislocation loop so generated is occasionally referred to as the “Hu” loop [17].

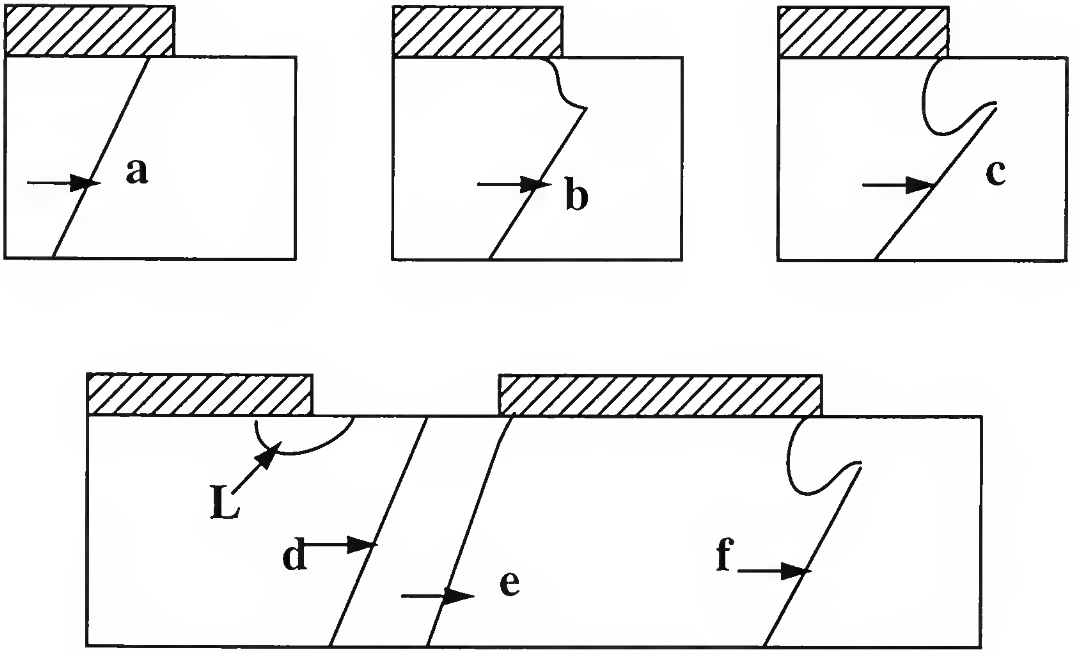


Figure 1.6 A frequently occurring mechanism of creation and trapping of dislocation loops through the interaction of a film edge induced stress field with a travelling dislocations. A gliding dislocation approaches the nitride edge (a), experiences the stress field induced force and begins to bend (b), (c), and continues to glide on after shedding a dislocation loop L (d), interacts attractively with the left side edge stress field (e), and repeats the cycle (f). [From reference 17]

The straddling configuration of the loop shown in Figure 1.6 is especially deleterious to devices like transistors. The travelling dislocation may continue to glide till it comes to its final position, determined by the macroscopic stress fields such as thermal stresses. This mechanism of defect generation has been frequently observed in devices using LOCOS as the isolation technique [18-20]. It also operates in the generation of "emitter-edge-defects" [16] through interactions with gliding thermal slip dislocations.

Stress from multiple and periodically patterned nitride stripes is studied using the finite element method in Chapter IV. The effect on point defects and extended defects is also presented. As the devices get scaled and the geometries get more complex, robust simulation of stress from thin films will become essential. The methodology developed to simulate such stresses encompasses a wide array of structures and provides both qualitative and quantitative insight into the physics.

1.2.3 Stress from Isolation Trenches

As new generations of integrated circuits evolve, two major trends are evident: the packing density on a chip increases, and device dimensions are reduced. Higher packing densities are achieved by making devices smaller and by packing them closer together. One prime requirement for these closely packed devices is the need for good electrical isolation. In general, as the area available for isolation has reduced the stress levels in the substrate have risen [21]. Also, as the active device regions are brought closer to the isolation structures, control of dopant diffusion in these regions becomes difficult.

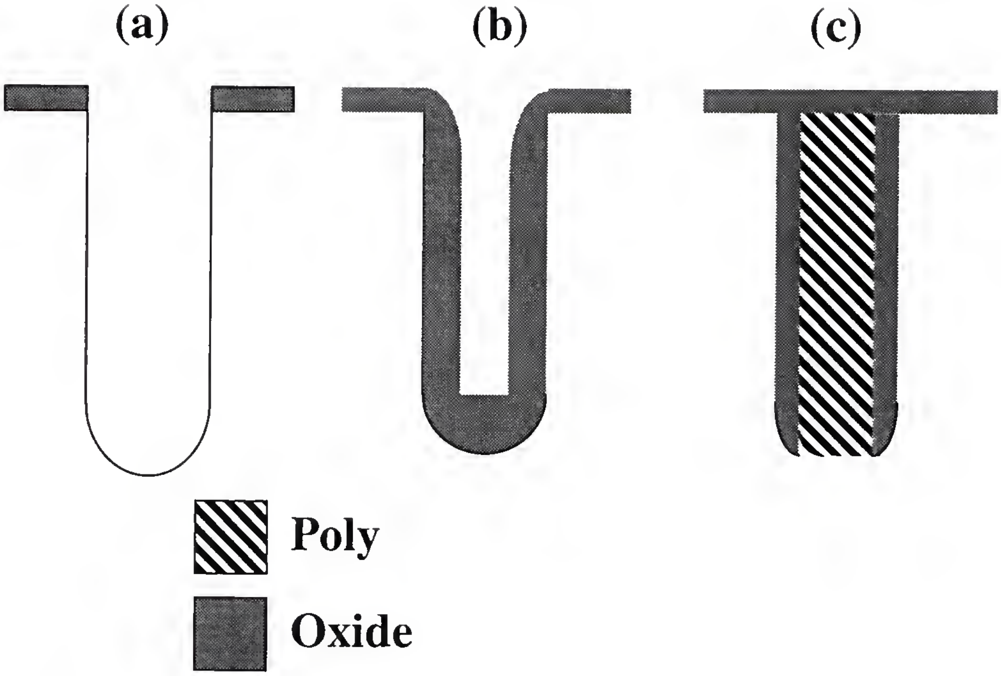


Figure 1.7 Deep trench fabrication sequence: (a) trench is formed by RIE, followed by (b) oxidation, and (c) removal of oxide at bottom of trench, filling with polysilicon, and planarizing. From reference 21.

Stress from isolation structures like trenches, and V-grooves has been investigated both experimentally [21, 22] and by using finite element analysis [23, 24]. Fahey et al. [21] pointed out the disadvantages of using low thermal budgets in the drive to form shallow junctions. The oxide, with a lower viscosity at these low temperatures, is unable to deform, thereby transferring an enormous stress on to the silicon substrate. Typically, reactive ion etching is used to form isolation trenches in silicon technology (Figure 1.7). A thin layer of thermal oxide is then grown on the trench sidewalls. The trenches are finally filled with Chemical Vapor Deposited (CVD) silicon dioxide or another CVD dielectric. CVD polysilicon, though not a dielectric, is frequently used in place of the CVD silicon dioxide. High levels of stress at the trench corners can be generated during thermal oxidation, though the use of very thin oxides can alleviate this problem. During thermal treatment thermal expansion mismatches between silicon and the trench-fill material can lead to significant stresses. For example, the thermal expansion coefficient of silicon dioxide is nearly an order of magnitude smaller than that of silicon. Intrinsic stresses of the CVD materials can also be a problem.

Hu [25] investigated and summarized [17] a large number of cases of stress from isolation techniques. He showed that for an oxide trench-fill that expands against the trench wall, a compressive stress component exists in a direction perpendicular to the trench sidewall. This stress is predominantly localized near the bottom part of the trench sidewall, and near the surface region. The stress component parallel to the trench sidewall, is generally tensile and localized near the center of the sidewall. The shear component of the stress is almost absent at the mid-length of the trench and becomes dominant only near the trench end.

1.2.4 Misfit Stress and Dislocation Generation in Epitaxial Silicon Wafers

A large lattice interfacial mismatch occurs when a lightly doped epitaxial (epi) layer is grown on top of a heavily doped substrate. For example, if the substrate is doped with $10^{18} \sim 10^{19}$ /cm^3 boron and the lightly doped epi has boron in concentrations of the order of 10^{15} /cm^3, a lattice mismatch of approximately 0.028 Å is present at the interface of the epi and the substrate [26]. The resulting stress that occurs during the CVD deposition of the epi is tensile on the epi side, while the substrate is in compression. If this stress is below a certain threshold, the system relaxes by wafer bowing, and if above it, dislocations are generated. A large wafer bow is undesirable from the lithographic view point, while the dislocations might cause yield related problems.

A part of the problem can be alleviated by a phenomenon called "compensation," where the heavily doped substrate is "grown" with a solute which causes the lattice constant of silicon to change. Lin et al. [26] demonstrated this concept by incorporating germanium during the wafer-melt process in the heavily doped substrate. As opposed to boron, germanium causes the lattice constant of silicon to increase. It was also determined that a germanium to boron concentration ratio of 6.8 could bring about complete compensation in the silicon lattice. The lightly doped epitaxial layer can then be grown on top of the boron doped substrate with minimal misfit at the interface.

1.2.5 Stress from Dislocation Loops

High dose ion-implantation is frequently used to define regions like the source and drain in a MOSFET, and the emitter regions of a bipolar transistor. Though this procedure controllably produces the desired doping levels and junction depths, it amorphizes the region it is implanted in. During subsequent annealing this amorphized region recrystallizes to form end-of-range dislocations at the original amorphous-crystalline interface. Unlike point defects, extended defects such as dislocation loops are large enough to be observed by techniques such as Transmission Electron Microscopy (TEM). Using this technique Jones et al. [27] analyzed the morphological characteristics of the extended defects due to ion-implantation in silicon. They observed a strong dependence on the species, dose and energy of the implant. The anneal characteristics were strongly governed by the time and temperature of the thermal cycle.

If uncontrolled, dislocation loops can affect the final properties of the device. A significant leakage current is known to exist if the dislocations are located across junctions[28]. If the dislocations are located outside the space charge regions, the device operation is not affected. Dislocation loops affect dopant redistribution during thermal cycling by capturing and emitting point defects. This might lead to major variations in junction depths. Dopant profiles in the device are also influenced by the stress field associated with the loops. A compressive stress field leads to an undersaturation of interstitials, thereby retarding diffusion of dopants like boron and phosphorus, which rely on interstitials for diffusion.

1.3 Organization

This work attempts to analyze and model stress effects in scaled silicon device technology. Based on the current understanding of point defects and their interaction with stress fields, an effort is made to identify critical stress inducing sources, model the characteristics of these sources and then apply the results to understand the effects on current and future semiconductor device technologies. This work also brings out the critical issues and limiting factors that affect modern process design. Relevant physics is incorporated wherever the need exists. Numerical simulations are resorted to for complex problems, and their results are qualitatively explained. Experimental verification is performed for most of the simulated data.

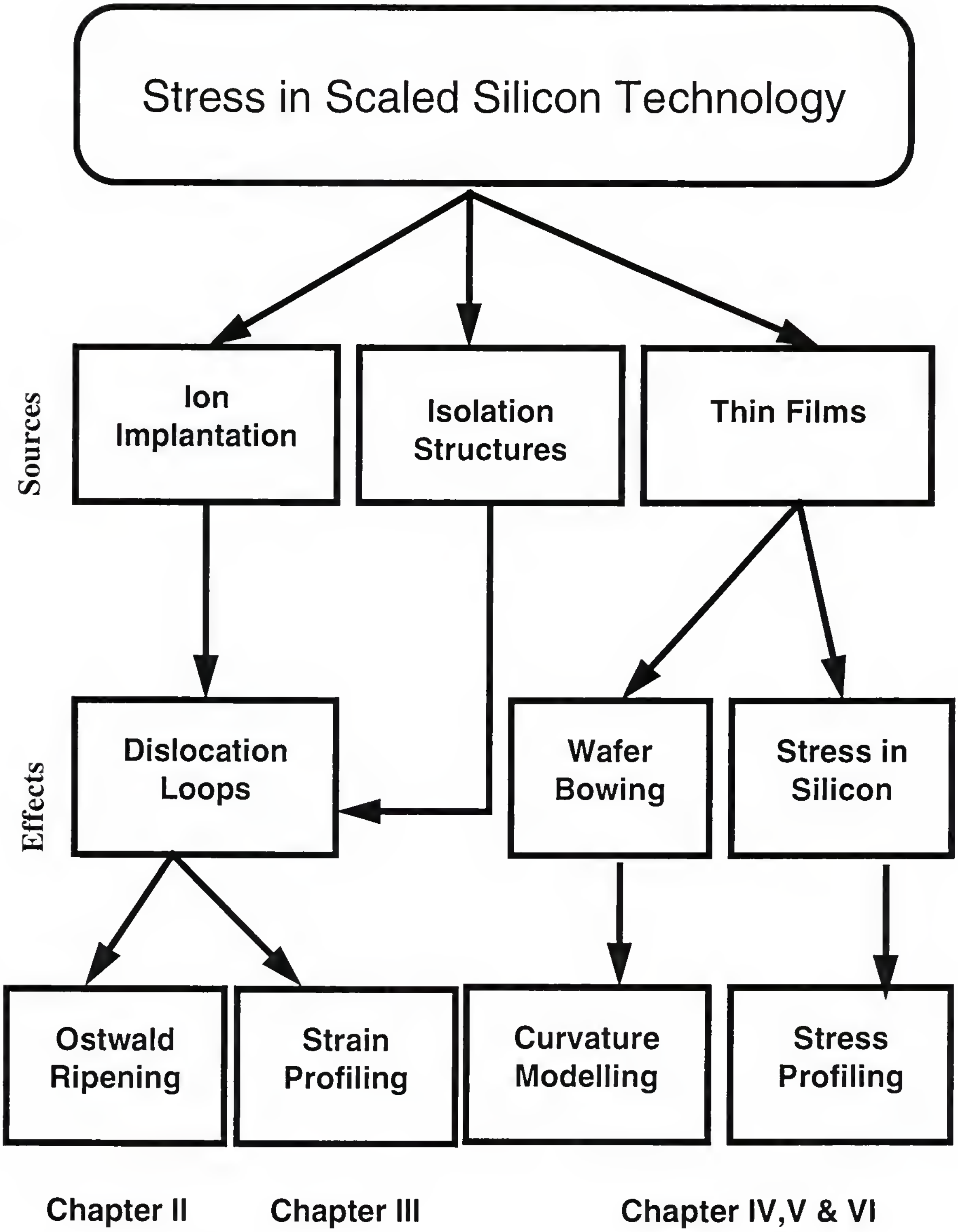


Figure 1.8 Stress effects in silicon studied as part of this dissertation.

Figure 1.8 illustrates the stress effects in scaled silicon technologies studied as part of this dissertation. The sources of stress are classified and studied as part of different chapters. Chapter II looks at the evolution of dislocation loops in an inert ambient. Since the loops affect dopant profiles, information about their size and density are important for a process engineer. This chapter develops point defect based two-dimensional models for the evolution of loops in an inert ambient. The Ostwald ripening process, where large loops grow at the expense of smaller ones, is the basis of the model developed. Loop evolution as observed under TEM analysis is used to verify the accuracy of the model. The model is subsequently used in Chapters III and VI.

Knowledge of the stress from a given dislocation loop ensemble is important for process modeling. There are two major consequences of this stress. First, it is the driving force for the movement of point defects into and out of the ensemble. Second, the stress can affect dopant diffusion in regions close to the ensemble. A model for stress due to the dislocation loops based on the widely used finite element analysis is developed as part of Chapter III. The effect of boundary conditions is studied, and the current status of the investigations brought out. X-ray rocking curve analysis is used to obtain peak values of strains in the substrate. These are then compared to the simulated values. The simulations provide the user with the means of profiling the stress in the substrate, not possible with the rocking curve experiments.

Stress from thin films is the focus of Chapter IV. The effect of multiple nitride stripes on the silicon substrate is studied. The stress in the bulk is characterized as a function of stripe width and thickness. The results of this chapter lay the groundwork for the design of the experiment for Chapter V and the simulation scheme of Chapter VI.

Wafer curvature due to lattice mismatch between epitaxial layers and the substrate is modeled and compared to available experimental data as a second part of Chapter IV. Large wafer bow is undesirable due to lithographic limitations. A phenomenon called "compensation," which has been successfully used to minimize the bow, is simulated. This provides the user with a predictive capability to optimize this process.

Based on the results of Chapter IV, an experiment is designed to investigate the effect of stress from patterned nitride stripes on point and extended defects in Chapter V. Phosphorus is used as a representative dopant to investigate the effect on point defects. High dose ion-implantation is used to introduce dislocation loops in the substrate. These loops are then annealed in the presence of the nitride stripes. Plan view TEM (Transmission Electron Microscopy) is used to extract the size and density characteristics of the dislocation loop ensemble. The results are analyzed and qualitatively explained. The experiment design includes splits on stripe widths and thicknesses, and anneal conditions, to bring out the corresponding dependencies.

Chapter VI quantifies the results of Chapter V. It integrates the models developed in this work and verifies them with the experimental data. The models for stress from Chapter IV are used to simulate the stress-assisted diffusion of phosphorus. The same models are integrated with loop evolution models (Chapter II), and loop stress models (Chapter III), to predict the stress-assisted evolution of ion-implanted dislocation loops. Experimental data from Chapter V and the work of other researchers is used to estimate the upper bounds for the fundamental parameters used to optimize the simulations. Using these extracted parameters the effect of stress on a scaled ULSI MOS device is simulated. The change in threshold voltage of the device as a function of the substrate stress is extracted using a device simulator.

Some of the important contributions of this work are summarized in Chapter VII. Based on the trends in modern ULSI technology some of the results are extrapolated with sound reasoning. Finally, some recommendations are made regarding possible future directions to the research in this field.

CHAPTER II
MODELING THE EVOLUTION OF DISLOCATION LOOPS IN AN INERT AMBIENT

The use of high dose ion-implantation, to obtain heavily doped regions in silicon such as the source and drain of a MOSFET, has gained immense popularity in the last two decades due to the inherent controllability of the implanted profile. However, the damage created in the substrate by this process strongly affects dopant redistribution during later anneals. During the anneal, solid phase epitaxial regrowth of the amorphized region leads to the formation of end-of-range dislocation loops at the amorphous/crystalline (a/c) interface. It has been shown that the end-of-range dislocation loops affect the distribution of point defects by the absorption of interstitials or emission of vacancies at their core boundary during growth and by the reverse process during shrinkage [29, 30].

Earlier work [31-34] established theoretical models for a single circular dislocation loop and its interaction with point defects. Bullough et al. [32] used Bastecka and Kroupa's [33] stress field solution to predict the migration of a single interstitial atom around a single dislocation loop. Borucki [34] proposed a model for the growth and shrinkage of a single dislocation loop due to the capture and emission of point defects, and simulated the point defect variation from an assumed initial high supersaturation around a periodic array of the loops in a three dimensional numerical solver of diffusion equations. Park, Jones, and Law [29] developed a statistically based model for loop growth in an oxidizing ambient, where the interstitials injected from the growing oxide contribute to the growth of the large loops. Pressure effects from the loops were incorporated into the point defect equations. Liu [35] demonstrated that in an inert ambient loop growth kinetics are mainly governed by loop-to-loop interactions, with the large loops growing at the expense of smaller ones (Ostwald ripening). This work quantitatively analyzes the size and density distribution of the loops as a function of anneal time and temperature.

2.1 Experimental Details

The experimental procedure was designed and executed by Liu [35]. Czochralski single crystal silicon wafers (<100> orientation, boron doped (1~100 Ω cm), 600~650 μm thick) were used as the starting material. Si^+ ions were implanted at 50 keV and a dose of $1x10^{15}/cm^2$ into the silicon substrate. The implant temperature was kept constant around room temperature and was stabilized during implantation using a way-flow freon cooled end-station. A dose rate of 20 μA was maintained throughout the implantation process. A continuous amorphous layer was formed as a result of the implantation. Upon annealing type-II or EOR (end-of-range) [27] dislocation loops were formed just below the amorphous/crystalline interface (~1200 Å deep), as determined by cross-sectional TEM measurements.

After implantation, the entire wafer was capped with 6000 angstroms of SiO_2 before the annealing process to limit any oxidation in the inert ambient. The wafers were then cut into four parts and annealed in a nitrogen ambient at 700, 800, 900 and 1000°C for times ranging from 15 minutes to 16 hours. The capped oxide for all samples was removed by HF before mechanical and jet etching. The total loop density, the average loop size, the loop distribution and the interstitials bound by loops were measured under plan view TEM on a JEOL 200CX TEM.

2.2 Experimental Results

The loop distribution N(r) versus loop radius r is shown for the various anneal conditions in Figure 2.1 to Figure 2.4. N(r) represents the loop density at radius r. A shift in the loop distribution towards a larger radius is observed with increasing time for each temperature. The velocity of this movement is smaller for the low temperature anneals. This is the result of the loop coarsening process. Since N(r) is proportional to r^2, the plot for large r is expected to show considerable scatter, particularly when the number of loops counted is relatively small, as in the case of the 1000°C anneal. If the temperature is kept constant, the loop size increases with anneal time, although at low temperatures (700-800°C) this movement is much slower than at high temperatures (900-1000°C). The total loop density decreases for increasing anneal time, causing the density of interstitials bounded by the loops to remain constant (at low temperatures) or to decrease (at high temperatures). For annealing times greater than 2 hours at 1000°C stacking faults are formed.

The average loop radius is measured for each anneal condition. Figure 2.5 shows the average loop radius versus anneal time at different temperatures. An increase in the average loop radius is observed with increasing anneal time, though this rate of increase is quite slow at the lower temperatures. At the early stage of the 700°C anneal, the loops are quite small. However, after 4 hours of annealing they are well developed. Also, with increasing anneal temperature, the average loop radius increases. This means that more of the implantation induced supersaturated interstitials move to the dislocation loops at the higher temperatures.

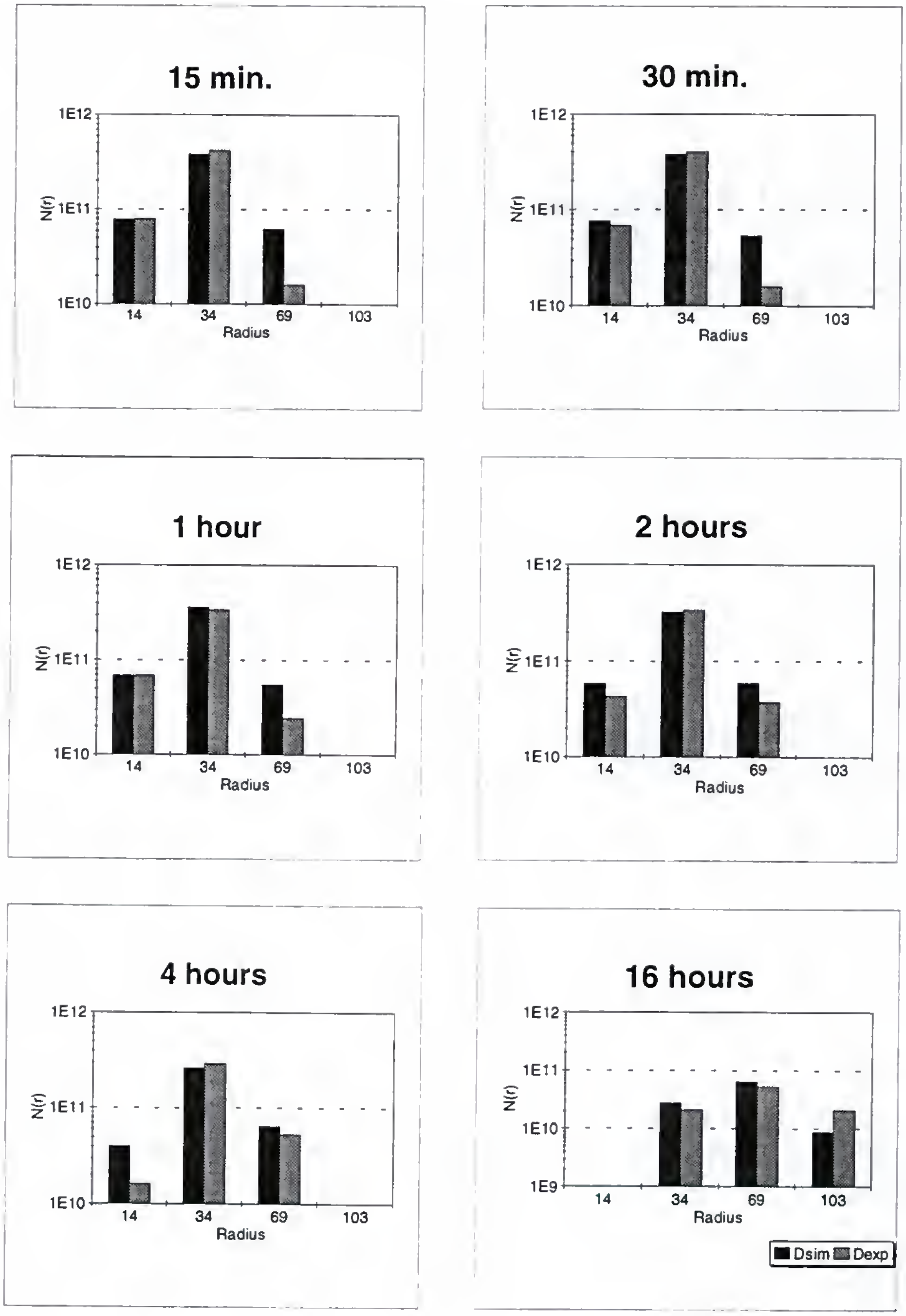


Figure 2.1 Size spectra of loops as a function of loop radius after annealing in nitrogen at 700°C for different anneal times. The radius is in angstroms and the density is /cm^2.

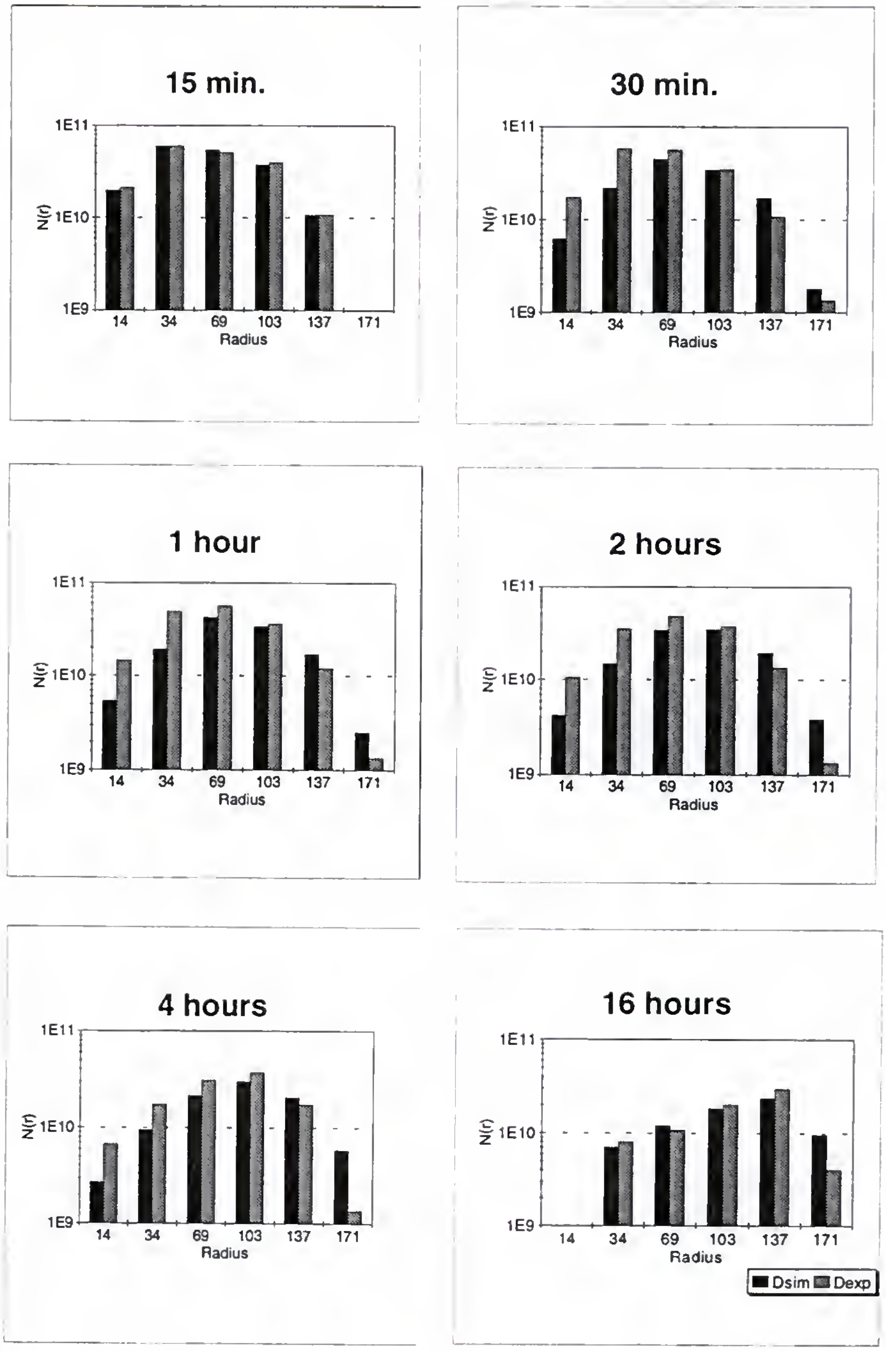


Figure 2.2 Size spectra of loops as a function of loop radius after annealing in nitrogen at 800°C for different anneal times. The radius is in angstroms and the density is /cm^2.

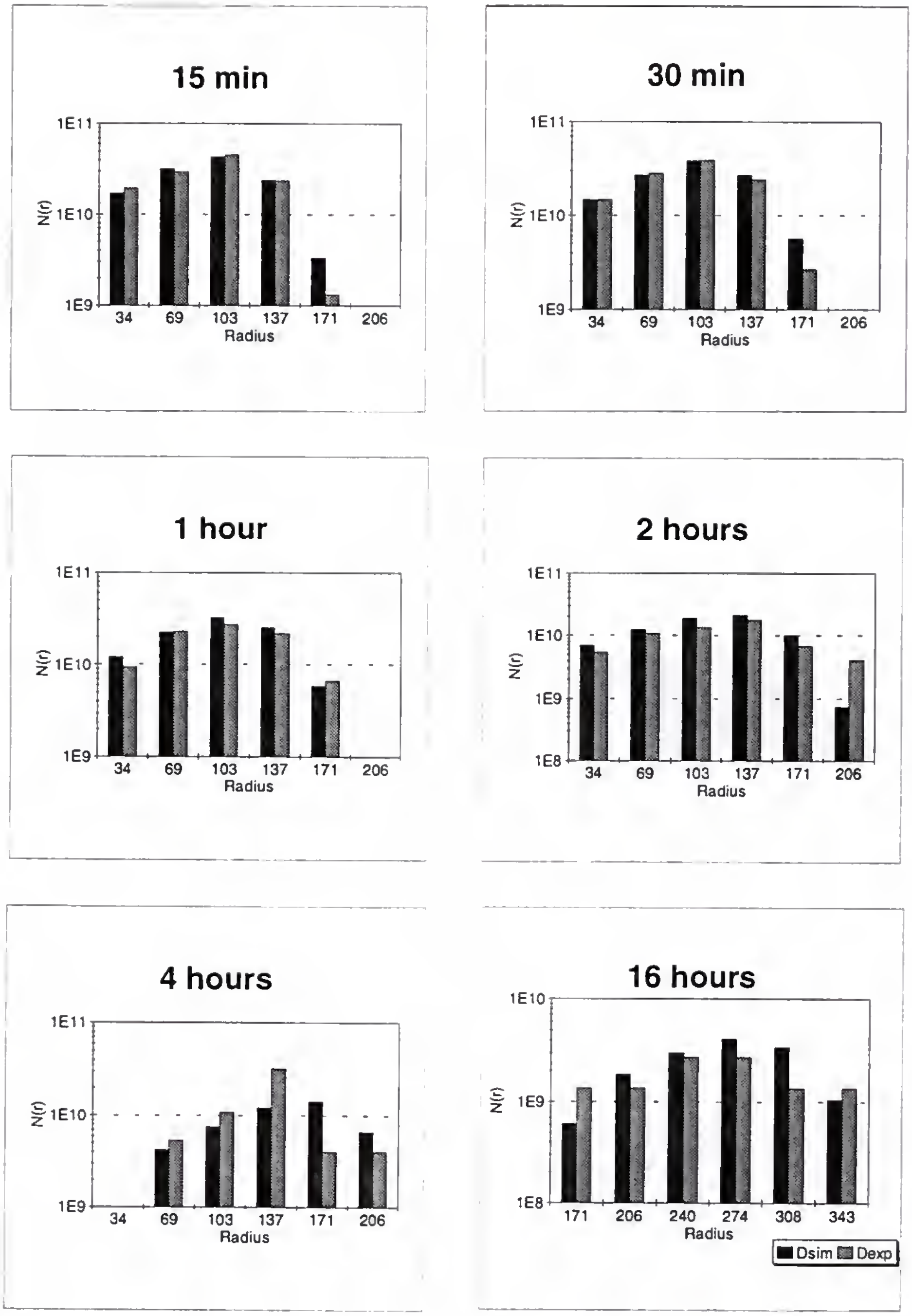


Figure 2.3 Size spectra of loops as a function of loop radius after annealing in nitrogen at 900°C for different anneal times. The radius is in angstroms and the density is /cm^2.

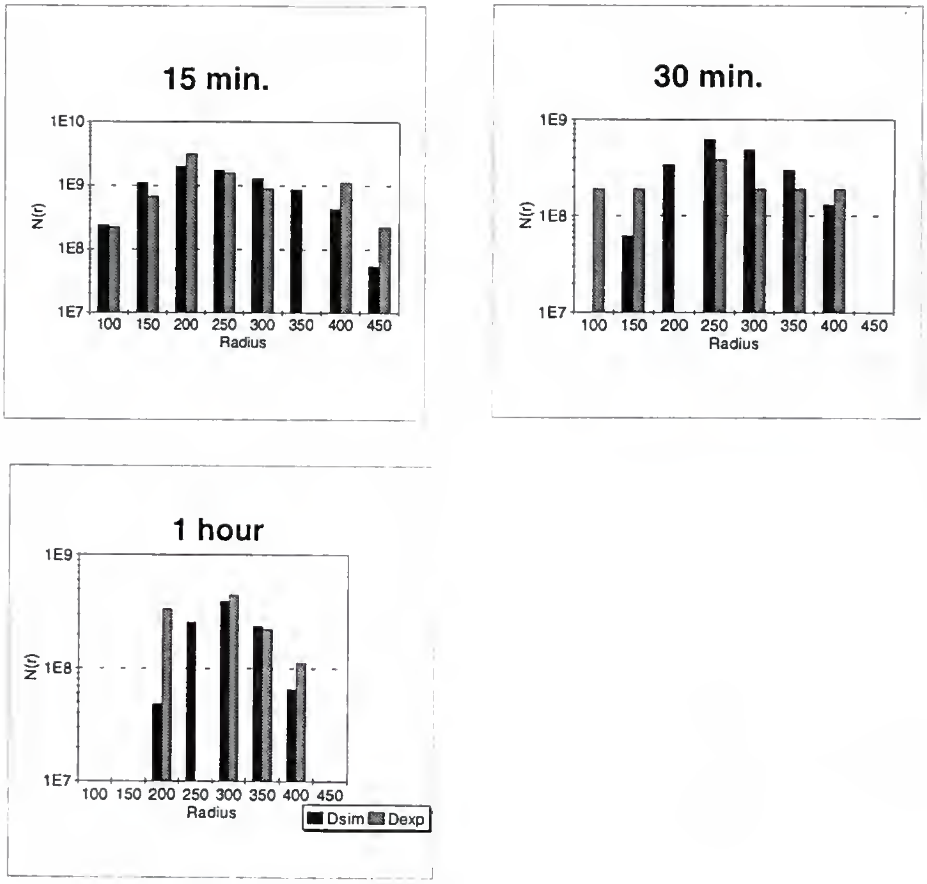


Figure 2.4 Size spectra of loops as a function of loop radius after annealing in nitrogen at 1000°C for different anneal times. The radius is in angstroms and the density is /cm^2.

The total loop densities are shown in Figure 2.6. A decrease in the densities is observed with increasing anneal time. If the anneal time is kept constant, the density is found to decrease with an increase in the temperature of the anneal. This implies that the initial rate of dissolution of the smaller dislocation loops is more pronounced at higher temperatures. At 1000°C the total density of loops after a 15 minute anneal is several orders of magnitude below the corresponding densities at the lower temperatures.

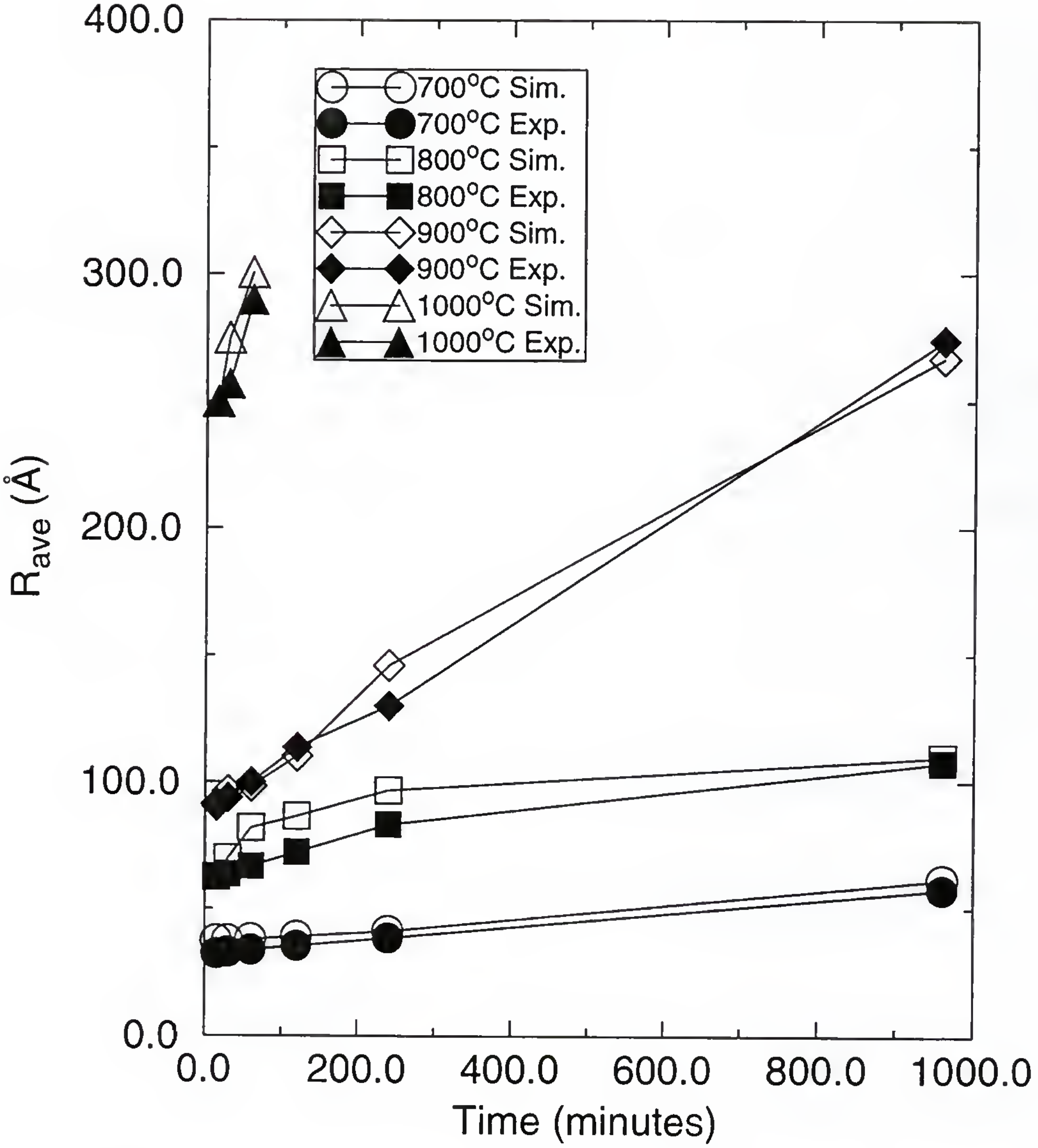


Figure 2.5 Plot depicting the increase in the average loop radius with increasing time for temperatures ranging form 700°C to 1000°C.

Loops begin their dissolution right after the 1000°C anneal. For the 700 and 800°C anneals, the loops remain in the coarsening regime and the densities of interstitials bound by the loops remain fairly constant. For the 900°C anneal, the density of the captured interstitials decreases with increasing time. However, the larger loops continue to grow, while the smaller loops continue to shrink and eventually dissolve.

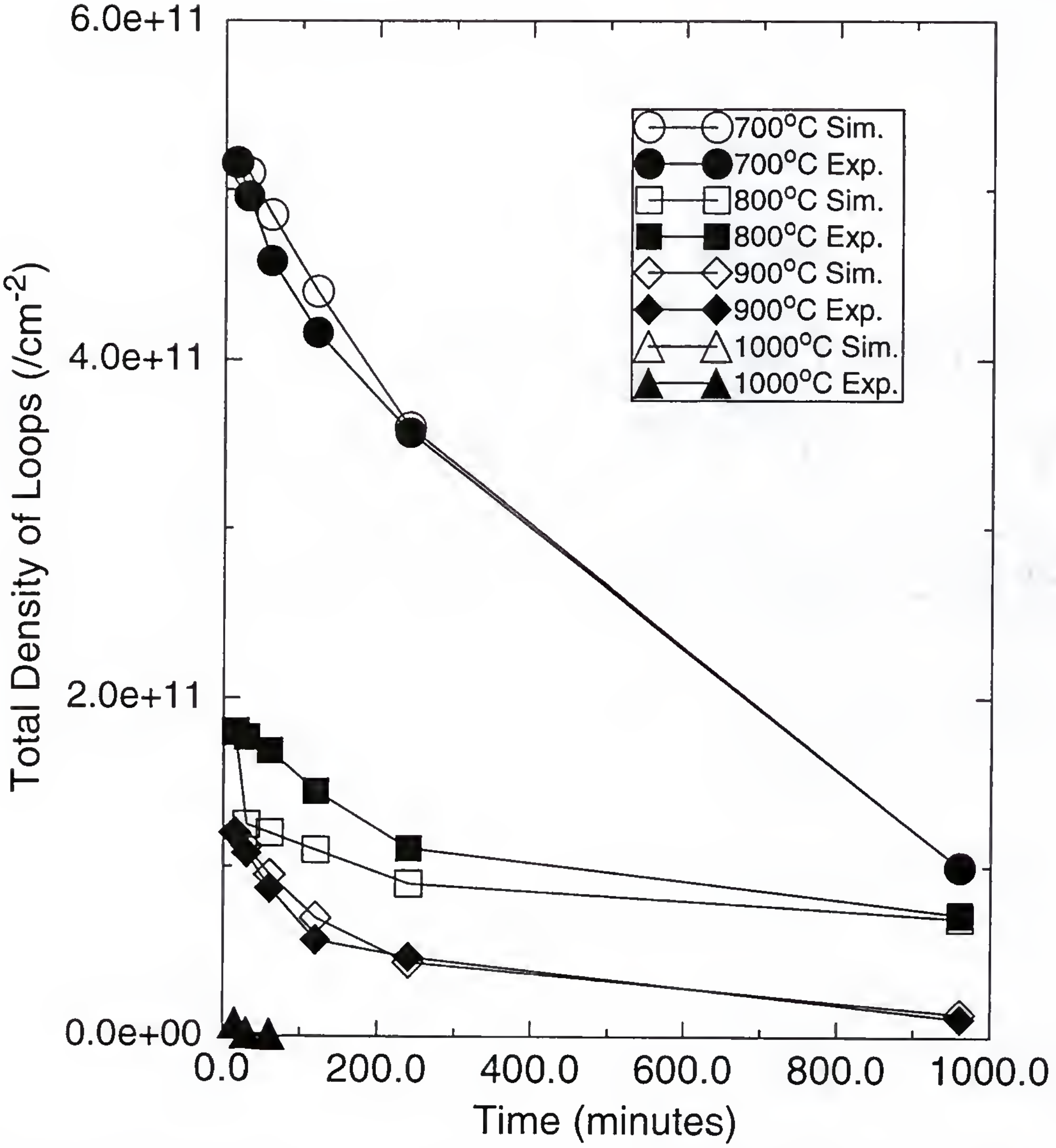


Figure 2.6 Experimental and simulated values of the total density of loops for various anneal conditions, showing the decrease in density of loops with increase in either time or temperature.

2.3 Modeling

The modeling strategy is a two-pronged one. A triangular distribution function model for the dislocation loop distribution is used from Park et al. [29]. The loop distribution is updated at each time step in the second part of the model by calculating the loss of trapped interstitials from the smaller atoms and using it to calculate the increase in size of the larger loops.

2.3.1 Modeling the Loop Distribution

As seen in the experimental data in Figure 2.1 to Figure 2.4, the loops distribution can be modeled in the form of an asymmetrical triangular distribution function. Such a model has been developed by Park, Jones and Law [29]. It assumes circular loops distributed on a plane interconnecting their centers. The orientation of the loops is assumed periodic in two perpendicular directions. The radius and density are assumed to follow an asymmetric distribution function. Each set of loop data is characterized by its minimum radius (R_{min}), its peak radius (R_p), where the density of the loops is a maximum (= D_p), and the maximum radius of the distribution (R_{max}). The total density of the distribution is represented by D_{all}. The unnormalized probability distribution function $f_d(R)$ is then given as

$$f_d(R) = \frac{2D_{all}(R - R_{min})}{(R_{max} - R_{min})(R_p - R_{min})} \quad \text{when } R_{min} < R < R_p \qquad \text{2-1}$$

$$f_d(R) = \frac{2D_{all}(R_{max} - R)}{(R_{max} - R_{min})(R_{max} - R_p)} \quad \text{when } R_p < R < R_{max} \qquad \text{2-2}$$

and the density at a particular radius $D(R)$ is given as

$$D(R) = \int_{R-\frac{\Delta R}{2}}^{R+\frac{\Delta R}{2}} f_d(R')dR' = f_d(R)\Delta R \qquad 2\text{-}3$$

The density D_p of the majority loops with radius R_p and its relation with the total density D_{all} can be expressed by using Equations 2-1 to 2-3:

$$D_p = f_d(R_p)\Delta R = \frac{2D_{all}\Delta R}{R_{max} - R_{min}} = \frac{2D_{all}}{m} \qquad 2\text{-}4$$

where m is defined to be $(R_{max} - R_{min})/\Delta R \equiv 2D_{all}/D_p$. The average radius for a given distribution is derived in Park et al. [29] as

$$R_{ave} = \frac{1}{3}(R_{min} + R_p + R_{max}) \qquad 2\text{-}5$$

This model is described in detail in reference 29. The model is extended and suitably modified to account for loop to loop interactions as observed in the experimental data. Growth and shrinkage of the dislocation loops are modeled in terms of their reaction with point defects at the loop layer boundaries. The boundary conditions are given by the reaction rates of dislocation loops and the point defect formation energy change due to loop growth or shrinkage. The interstitial continuity equation in the presence of dislocation loops is derived in Park et al. [29] and is used the current model as well. It incorporates the variation in the local point defect concentrations due to emission and/or absorption of interstitials/vacancies by the dislocation loop ensemble.

2.3.2 Modeling Mechanisms of Loop Growth

Growth of loops during a thermal anneal occurs via two main mechanisms [36]. The first occurs via the migration of point defects to and from loops, and is called the bulk diffusion mechanism. The second mechanism is due to the glide and self-climb of loops resulting in the aggregation and coalescence of loops.

When the bulk diffusion mechanism is operative, loop growth or shrinkage occurs by the diffusion of point defects to and from the loops via the substrate. For the case of ion-implanted silicon the point defects that migrate are interstitials. The diffusion limited change in loop radius, r, is then $dr/dt = AD_I grad(C_I)$, where A is a geometrical factor depending on the boundary conditions for diffusion, D_I is the diffusivity of interstitials, and C_I is the concentration of interstitials.

The driving force for aggregation of loops by a combination of glide and self-climb is provided by the elastic interaction existing between the loops. In this case a loop of radius r_1 glides towards a loop of radius r_2, $r_2 > r_1$, and coalesces with it to form a larger loop.

The annealing behavior of type-II dislocation loops follows the Ostwald ripening process of loop coarsening governed by a bulk diffusion phenomenon [35, 36]. In this process the smaller loops shrink and eventually dissolve, while the larger loops absorb the emitted interstitials and increase in size. Physically, this is because it is energetically more favorable for a larger loop to increase in size and a smaller loop to dissolve.

The effective local equilibrium concentration of interstitials at the loop layer boundary, C_{Ib}, is given [34, 37] as

$$C_{Ib} = g_{bc}C^*_{I(P)}\exp(-\Delta E_f/kT) \qquad 2\text{-}6$$

$$C_{Vb} = g_{bc}^{-1}C^*_{V(P)}\exp(\Delta E_f/kT) \qquad 2\text{-}7$$

where g_{bc} is a geometric factor (≅0.3), $C^*_{I(P)}$ is the pressure dependent concentration of interstitials, k is the Boltzman's constant and T is the absolute temperature. ΔE_f is the change in defect formation energy due to the self-force of a dislocation loop during the emission and absorption process at its edge:

$$\Delta E_f = -\frac{\mu b\Omega}{4\pi(1-\nu)R}\left[\ln\left(\frac{8R}{r_c}\right)-\frac{2\upsilon-1}{4\nu-4}\right] \qquad 2\text{-}8$$

where μ is the shear modulus, b is the magnitude of the Burgers vector of the loop, Ω is the atomic volume of silicon, r_c is the core (torus) radius of the loop, υ is the Poisson's ratio, and R is the radius of the dislocation loop. According to Equation 2-6, the concentration of self-interstitials at the periphery of a dislocation loop of radius r_1 is lower than that at the periphery of a loop of radius r_2, when $r_1 > r_2$ (Figure 2.7). Therefore, a gradient in the concentration of self-interstitials is established between dislocation loops with different radii. This concentration gradient induces a self-interstitial flux from the smaller loops to larger ones. As a result larger loops grow and smaller loops shrink until they eventually vanish, in accordance with the Ostwald ripening phenomenon. This constitutes the dislocation loop coarsening process.

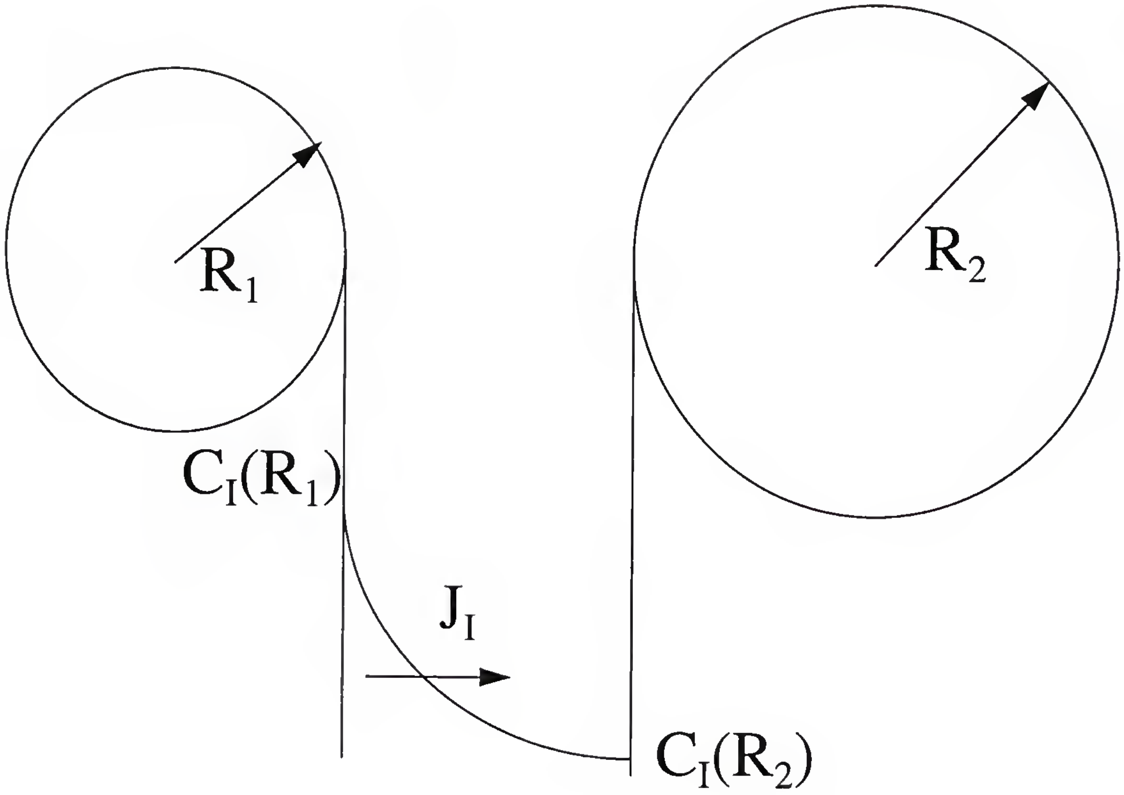


Figure 2.7 Schematic diagram to illustrate the silicon self-interstitial concentration gradient established due to the size difference of the dislocation loops.

The radii and the density of the majority sized loops (or the unit distance L_p between the loops) can be correlated with the number of silicon atoms bound by the dislocation loops per unit area ($n(R_p)$) by considering that the density of majority size loops D_p is equal to 0.5 L_p^{-2}:

$$n(R_p) = (0.5 \cdot \pi n_a R_p^2)/L_p^2 \qquad 2\text{-}9$$

where n_a is the atomic density of Si atoms on the <111> plane (=1.5 x 10^{15} cm^{-2}). If n, is the density of interstitials bound at radius R of the ensemble, its time derivative should equal the absorption of interstitials or the emission of vacancies at the loop layer boundaries, i.e.

$$\left.\frac{\partial n}{\partial t}\right|_{atRadiusR} = \alpha K_{IL}(C_I - C_{Ib}) - \alpha K_{VL}(C_v - C_{Vb})\Big|_{atRadiusR} \qquad \text{2-10}$$

where α is an effective cross section of the loop layer in the unit of linear length, K_{IL} is the constant of reaction between the interstitials and the dislocation loop collection, K_{VL} is a similar constant for vacancies, $C_{I/V}$ is the concentration of interstitials/vacancies, and $C_{Ib/Vb}$ are defined in Equations 2-6 and 2-7. It is apparent that during the coarsening process the smaller loops loose silicon atoms to the larger ones. Thus the quantity on the left in Equation 2-10 should be positive above a certain value of the radius (R_{crit}), and negative below it, i.e.

$$\frac{\partial n}{\partial t} > 0 \text{ for } R > R_{crit} \qquad \text{2-11}$$

$$\frac{\partial n}{\partial t} < 0 \text{ for } R < R_{crit} \qquad \text{2-12}$$

Such results were confirmed using simulations in FLOOPS (Florida Object Oriented Process Simulator). In this model the net loss of silicon atoms at an average size (= $(R_{min} + R_p)/2$) is estimated, and used to calculate the rate of growth of the loops of radius R_p, i.e.

$$\left.\frac{\partial n}{\partial t}\right|_{R_p} = \left.\frac{\partial n}{\partial t}\right|_{\frac{R_{min}+R_p}{2}} \qquad \text{2-13}$$

The relationship between the time derivatives of R_p and n is derived as

$$\left.\frac{\partial n}{\partial t}\right|_{R_p} = \left[\frac{\partial n}{\partial R_p} + \frac{\partial n}{\partial L_p} \cdot \frac{dL_p}{dR_p}\right]\left(\frac{\partial R_p}{\partial t}\right) \qquad \text{2-14}$$

where the first two derivatives on the right are evaluated using Equation 2-9. Thus, Equations 2-13 and 2-14 give the time rate of change of the peak radius, which is then used to obtain the time rate of change of the other distribution parameters from empirically observed relationships as described by Park, Jones, and Law [29]. The distribution parameters were extracted at each time step, and corresponding density histograms ($N(r)$) were derived from them to plot with the experimental data (Figure 2.1-Figure 2.4). The major parameter in fitting this model to the data is K_{IL} (in units of second^{-1}), and is extracted as

$$K_{IL} = 1.6x10^{7}\exp(-1.01/kT) \qquad \text{2-15}$$

Physically, this determines the rate at which the interstitials react with the dislocation loop ensemble. At its high extremity, any concentration of interstitials above the equilibrium value reacts with the loops, and the reaction is purely diffusion limited. The corresponding constant for vacancies (K_{VL}) is zero in the simulations.

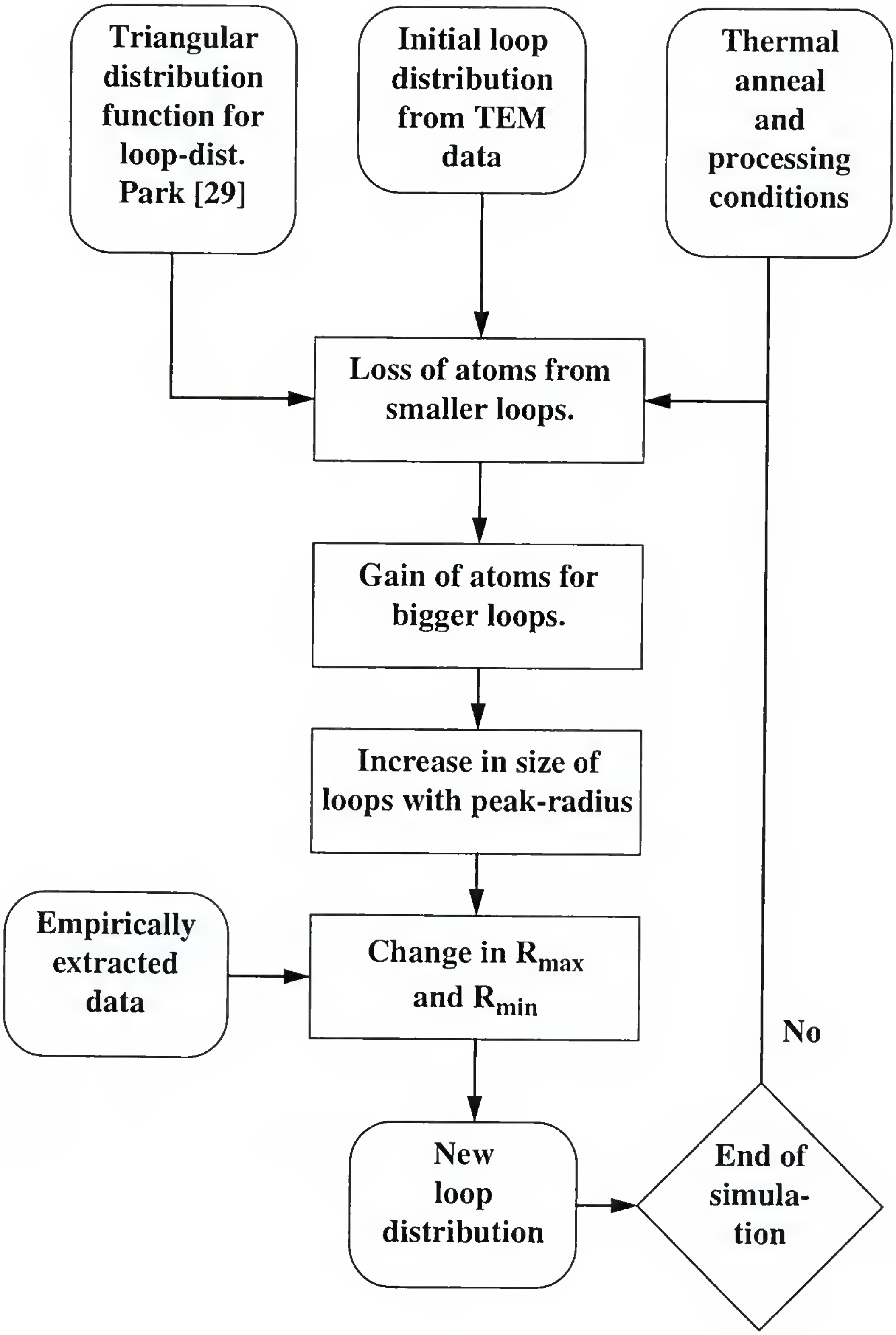

Triangular distribution function for loop-dist. Park [29]
Initial loop distribution from TEM data
Thermal anneal and processing conditions
Loss of atoms from smaller loops.
Gain of atoms for bigger loops.
Increase in size of loops with peak-radius
Empirically extracted data
Change in R_{max} and R_{min}
No
New loop distribution
End of simula-tion

Figure 2.8 Schematic to illustrate implementation of Ostwald ripening phenomenon.

The simulation results match the experimental data for most anneal conditions, indicating that the loop coarsening phenomenon is well modeled. For 700°C minor variations exist in the height of the histograms for anneals upto 16 hours. However, the total density (Figure 2.6) of the loops matches the experimental values at this temperature. The simulated and measured bin sizes for the 900°C anneal are also in agreement. At 800°C the model predicts a slightly higher initial dissolution rate of the loops, which results in small differences in the experimental and simulated bin sizes. Variations in bin sizes for the experimental and simulated cases diminish if two adjacent bins are added and plotted together. Such an assumption is valid due to a strong possibility of scatter in the TEM measurements. This also accounts for the differences in the bin sizes at 1000°C, where large scattering is observed in the experimental data. It should be noted that efforts to model the initial distribution of loops by an asymmetric distribution function for the 15 min./1000°C case lead to some errors which are propagated as the simulation progresses. However, the simulated total density of the loops is close to what is seen in the experimental data.

Simulated values for the average radius are plotted along with the experimental values in Figure 2.5. As seen, the model correctly predicts the average value of the radius for most anneal conditions.

2.4 Two-Dimensional Growth of Loops Under a Nitride Mask

The kinetics of dislocation loop evolution in ion-implanted silicon are strongly sensitive to the anneal ambient, which is either inert or oxidizing. It is well known that oxidation injects interstitials into the silicon substrate. The presence of these extra interstitials can lead to a sharp increase in dislocation growth rates; in some cases swamping out the growth due to the Ostwald ripening phenomenon discussed in the previous section. The growth of loops in an oxidizing ambient was studied in [29]. This section illustrates a simulation example of combining the two loop growth models into one simulation.

Common processing conditions used in semiconductor fabrication involve the use of a nitride mask. For example, during the growth of isolation oxides, a nitride is used as a mask for oxidation to prevent the oxide from growing in the active areas. Figure 2.9 illustrates the use of a nitride mask in the LOCOS isolation scheme. The loops under the growing oxide are expected grow at a much faster rate than under the nitride. For the anneal times considered, the loops under the nitride showed almost no growth in the simulations.

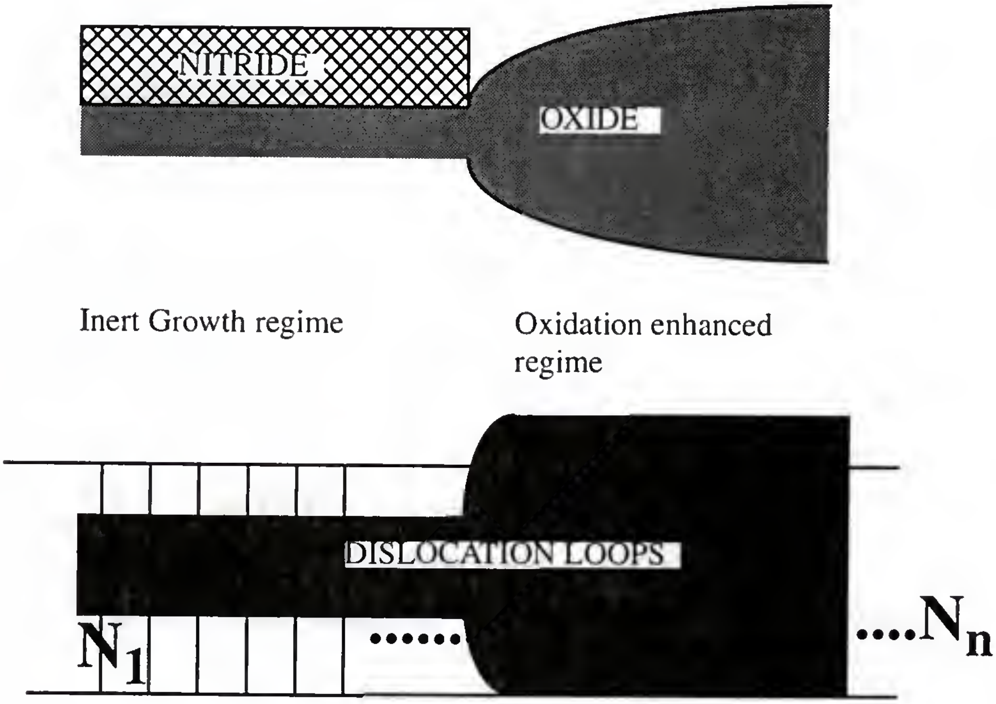


Figure 2.9 Growth of dislocation loops under inert and oxidizing regimes.

As illustrated in Figure 2.9, the loops grow faster under the isolation oxide. Each node (N_1 to N_n), is assigned a probability distribution function. The local interstitial concentration is considerably larger under the oxide (Figure 2.10). The dip in the plot at the dislocation loop core is due to the compressive component of the hydrostatic pressure introduced in the substrate by the loops (Chapter III). This leads to undersaturation of interstitials in that region.

The two-dimensional model is implemented in Florida Object Oriented Process Simulator (FLOOPS). The output from the simulator is shown in Figure 2.11.

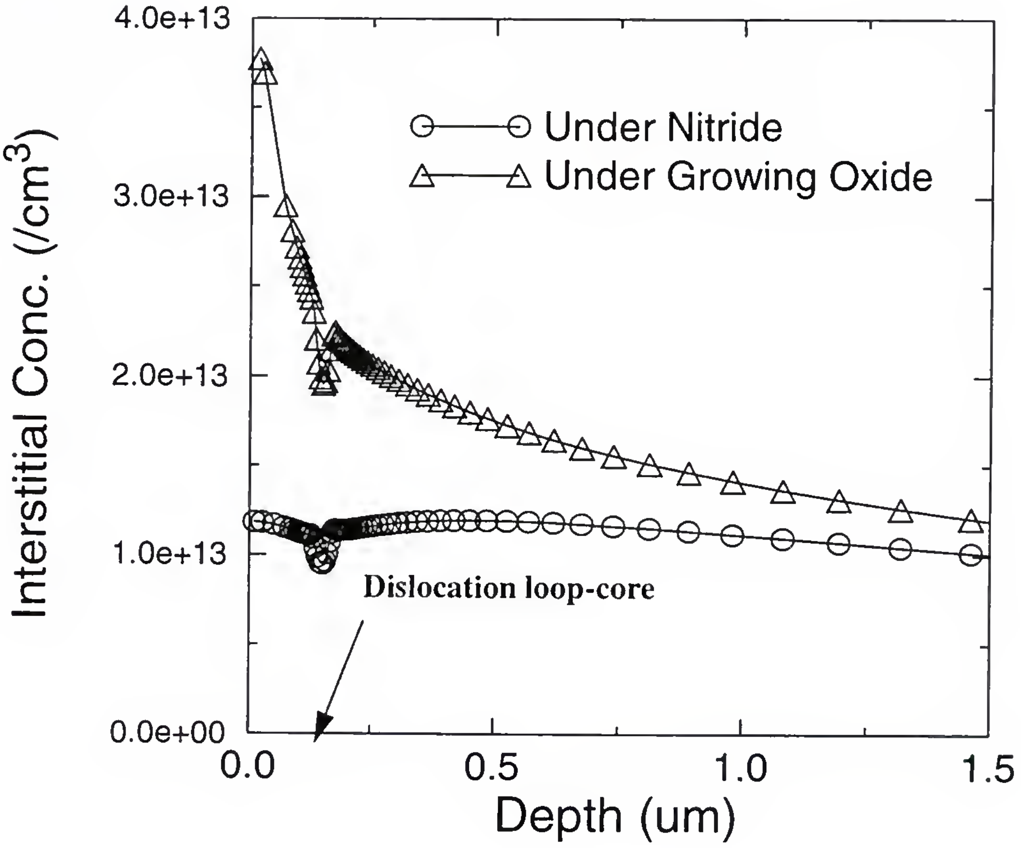


Figure 2.10 Interstitial concentration under the growing oxide and the nitride mask. The excess interstitials under the oxide cause the loops in that region to grow faster.

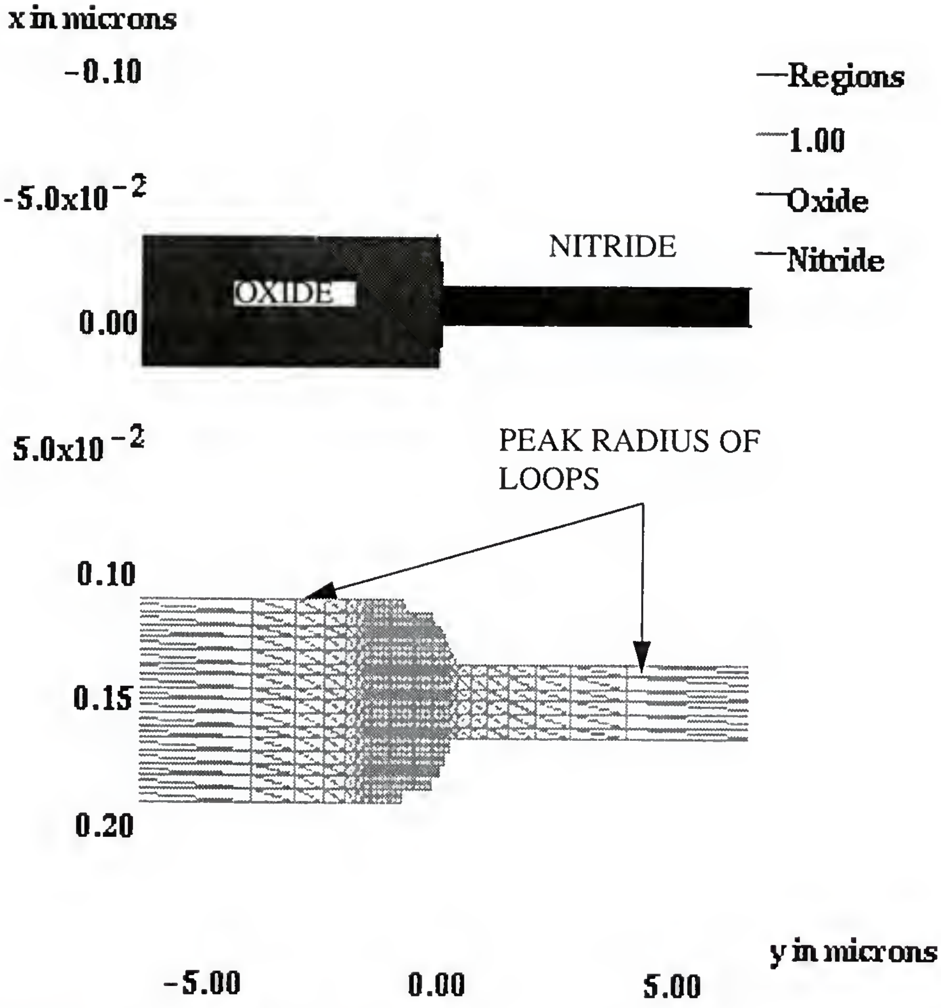


Figure 2.11 FLOOPS simulation showing the lateral variation of the peak-loop radius after a 2 hour, 900°C anneal in dry oxygen.

2.5 Summary

A plan view TEM study of the evolution of dislocation loops in silicon during annealing has been presented. It is shown that with increasing anneal time the average size of the loops increases while the total density of the distribution decreases. The same effects are observed with increasing temperature if the anneal time is kept a constant. At

1000°C stacking faults are formed beyond 2 hours of annealing. The loop evolution is shown to follow the Ostwald ripening phenomenon with the large loops growing at the expense of smaller ones.

A point defect based model which physically accounts for loop-to-loop interactions is developed from Park, Jones, and Law's [29] model. It correctly predicts the evolution of loops for most anneal conditions. Constants which define the rate of reaction between the loops and point defects are extracted for the 700-1000°C temperature range.

CHAPTER III
A TWO-DIMENSIONAL MODEL FOR STRAIN IN ION-IMPLANTED SILICON

Type-II end of range dislocation loops are formed under common implant and anneal conditions used in ULSI circuit fabrication. They affect dopant redistribution and can subsequently alter the electrical properties of the device. To design devices for optimal performance, it is important to predict the interaction between dopant atoms and dislocation loops. It has been proposed that the strain associated with these loops is the driving force for dopant diffusion during annealing [38-40]. An understanding about the source and magnitude of this strain is essential for process engineers designing devices for optimum performance. The loop strain is found to be a strong function of dislocation loop size and density, which changes during the anneal [41, 42]. A comprehensive model should take into account both the evolution of the loops and the strain. Such a model would be a useful tool for the device technologist.

In the past, Transmission Electron microscopy (TEM) has been used to characterize the evolution of extended defects under a wide range of anneal conditions [29, Chapter II]. While TEM can give adequate information about loop evolution, it does not provide any direct information on the strain fields associated with these defects. Recently, the technique of High Resolution X-Ray Diffractrometry (HRXRD) has been developed for the analysis of strain in ion-implanted semiconductors [41-43]. It allows for the strain and defect analysis to be performed on the same sample.

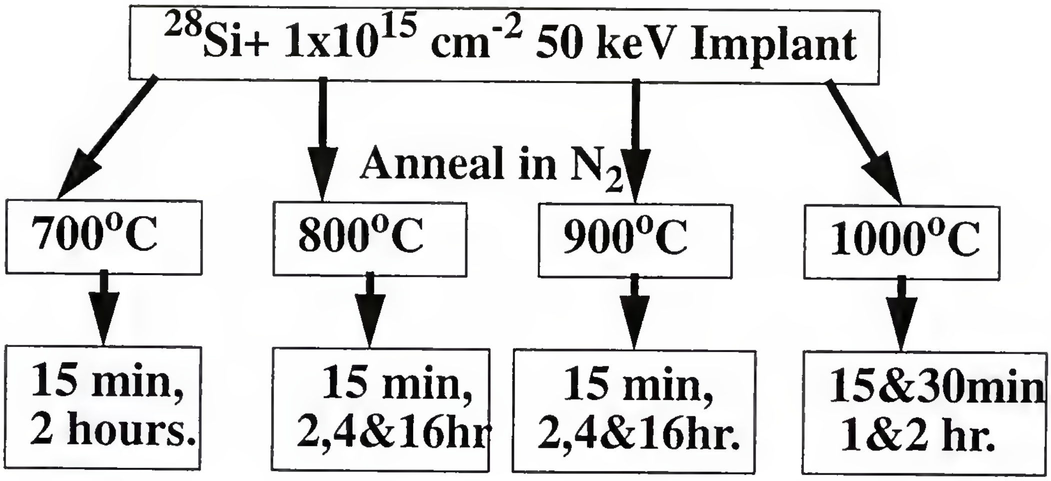


Figure 3.1 A matrix of the samples prepared and analyzed in this study.

In this study, a comprehensive two-dimensional numerical method is developed to model loop evolution (verified by the TEM data), and the resultant strain (verified using the HRXRD data). Additionally, the model predicts stress versus depth profiles in the substrate, not available from the x-ray analysis.

3.1 Experimental Details

The experimental procedure was designed and executed by Thompson [41]. The experiments were conducted using <100> Czochralski grown silicon wafers. These wafers were p-type (boron doped) with a resistivity of 5-10 Ω-cm, a diameter of 76 mm, and a thickness of 356-406 μm.The wafers were implanted with $1\text{x}10^{15}$ $^{28}\text{Si}^{+}/\text{cm}^{2}$ at an energy of 50 keV using a Varian ion-implanter. The ion beam was kept at a minimal current to reduce possible heating of the sample. After implantation a 5500 Å SiO_2 was deposited on the wafer to prevent any oxidation during the annealing process. The wafers were cleaved into approximately 1 cm^2 pieces for annealing and subsequent x-ray analysis. The samples were annealed in a N_2 ambient at 700°C, 800°C, 900°C, and 1000°C for times varying from 15 minutes to 16 hours. The annealing conditions are outlined in Figure 3.1. After the anneal, the surface oxide was removed from all samples using a buffered oxide etch for 5 minutes. The samples were tested for the presence of any residual oxide, which might effect the intensity of the x-ray peaks and/or introduce strain in the sample.

The fundamental result from the HRXRD is a rocking curve. A rocking curve is an angular x-ray scan around the Bragg diffraction-spot of a particular crystallographic plane. It plots the diffracted intensity around the Bragg angle; the collected intensity being limited by the geometry of the system. For most systems, the "rocking" is performed by moving the sample through the Bragg angle. If a layer of different lattice parameter is present, either on the surface or underneath it, two peaks will be evident in the rocking curve. One peak represents the substrate while the other peak indicates the presence of the strained layer. The separation between these peaks provides the difference in lattice parameter between the layer and the substrate. From a combination of different scans and from TEM data, the strain and/or relaxation in the system can be determined. Further details about the x-ray analysis are available in Thompson [41].

3.2 Experimental Results

The loop evolution, in an inert ambient, is observed using TEM microphotographs. The average loop radius is measured for each anneal condition, and is plotted as a function of the anneal time and temperature in Figure 3.2. It increases with anneal time, though the growth rate is small at low temperatures. It is also apparent that for a fixed anneal time the average loop radius is greater for the higher temperature anneals. The loops are quite small during the early stage of the 700°C anneal. The increase in the average radius of the loops above 800°C is associated with Ostwald ripening of the loops. This process was discussed and modeled in Chapter II.

The change in the total loop density, as a function of the anneal conditions, is shown in Figure 3.3. A decrease in the density is observed with increasing anneal time for most cases. If the time is kept constant, the density is found to decrease with an increase in temperature. This is the result of the loop coarsening process, during which the larger loops grow at the expense of smaller ones, which eventually dissolve. For the 700°C anneal the density remains fairly constant during the first two hours of the anneal.

The sharp drop in the number of trapped interstitials in the first two hours of the 1000°C anneal indicates that the loops are in a dissolution regime at this temperature. For the 800°C and 900°C anneals, the loops remain in the coarsening regime and the densities of interstitials bound by the loops remain almost constant (Figure 3.4).

The peak strain in the silicon lattice, from both the experiments and simulations (Section 3.3), is plotted in Figure 3.5. The change in the magnitude of this strain with time is minimal for the lower temperature anneals. However, at higher temperatures (1000°C) there is a sharp drop in its magnitude during the first two hours of the anneal. It appears that the magnitude of the strain is sensitive only to the anneal temperature for temperatures below 900°C. However, at elevated temperatures (> 900°C), it is a strong function of both the time and temperature of the anneal.

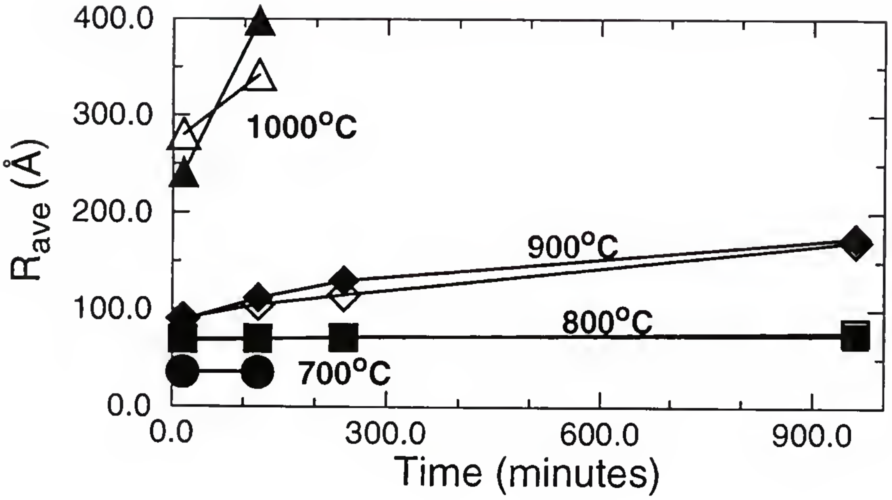


Figure 3.2 Experimental (filled) and simulated (empty) size of the average loop radius for various anneal conditions. At low temperatures the loops are small and the growth rate is not very pronounced. At higher temperatures, the small loops dissolve and the freed interstitials aid in the growth of the larger loops.

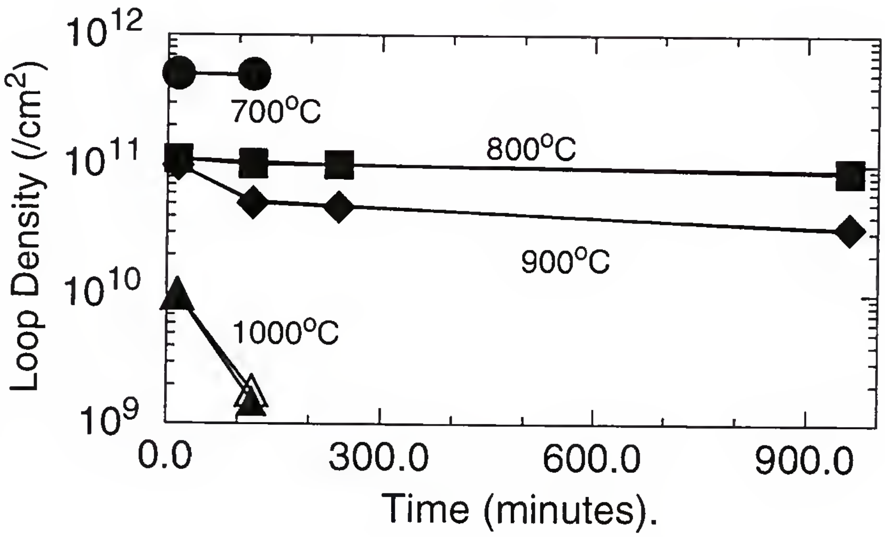


Figure 3.3 Experimental (filled) and simulated (empty) values of the total density of loops for various anneal conditions. The sharp drop in the density for the 1000°C anneal is representative of the loop dissolution process. Coarsening of loops is evident for the 800-900°C anneals.

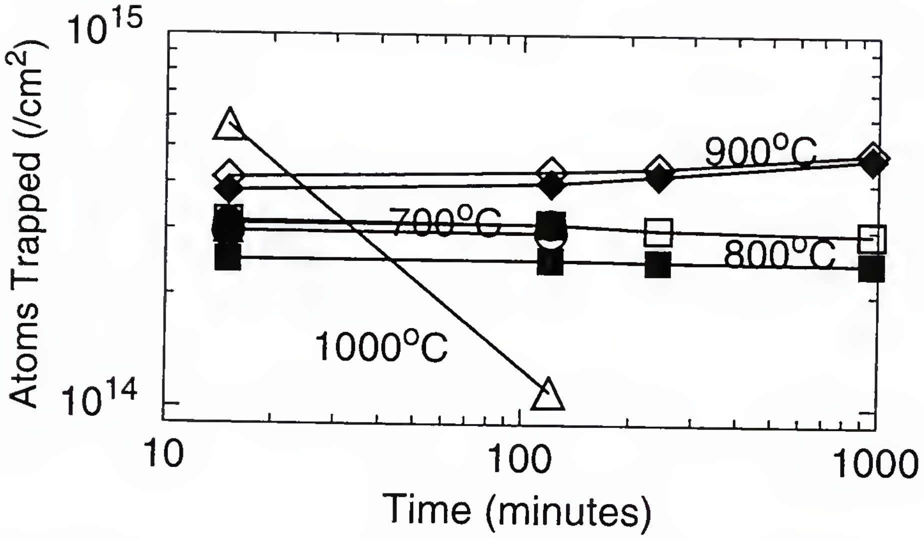


Figure 3.4 Experimental (filled) and simulated (empty) values of the captured interstitial dose for various anneals. The implantation induced interstitials coalesce to form dislocation loops and are responsible for the strain in the crystal.

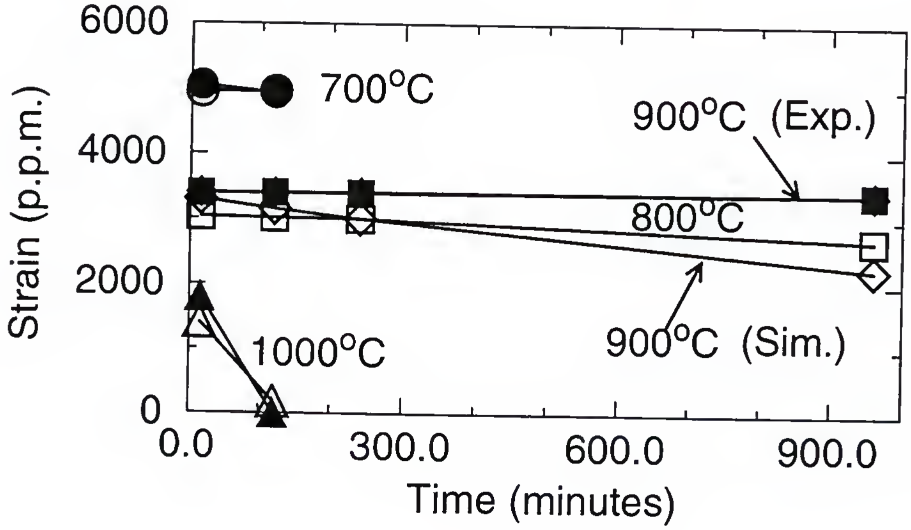


Figure 3.5 Experimental (filled) and simulated (empty) values of peak strain for various anneals. The dissolution of loops for the 1000°C anneal clearly reflects itself in the sharp drop in the strain at that temperature.

3.3 Modeling

As observed in the experimental data, the strain and the dislocation distribution in the silicon lattice are strongly coupled. This implies that a predictive model should incorporate this coupling. In this approach, loop evolution, as observed in the TEM microphotographs, is simulated using the Ostwald ripening models discussed in Chapter II. A model for strain, based on the number of atoms trapped by the loop ensemble, is developed and used at each time step of the simulation as an input to the Ostwald ripening model. A flow schematic of the modeling methodology is shown in Figure 3.6, and illustrates the coupling between the strain and loop distribution properties.

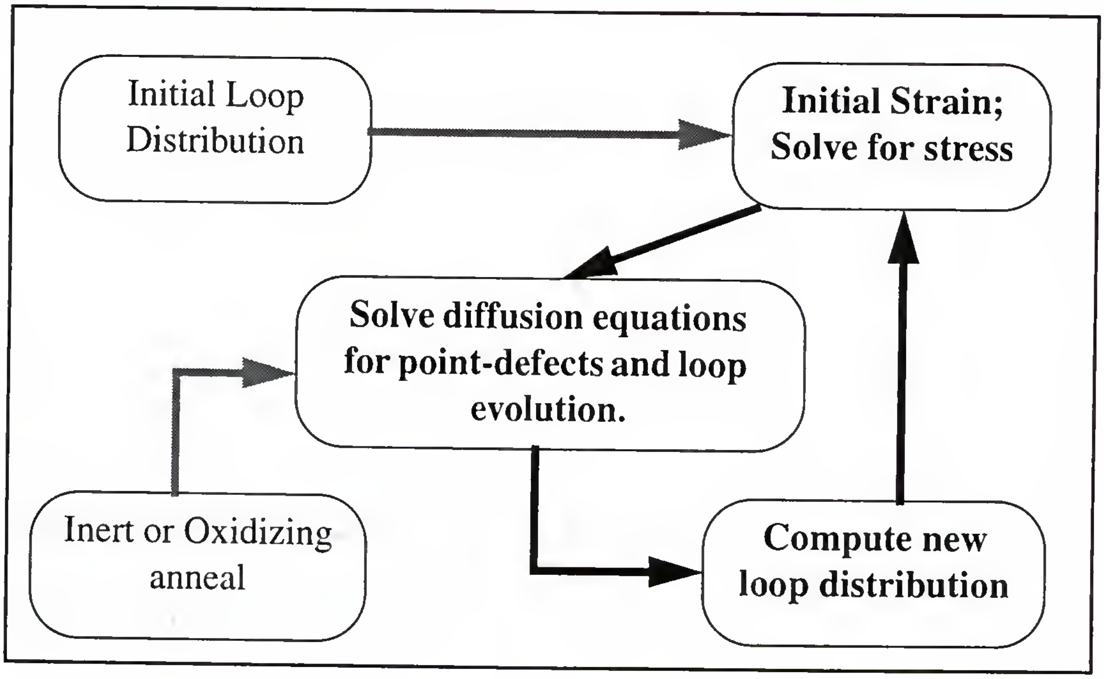

Initial Loop Distribution
Initial Strain; Solve for stress
Solve diffusion equations for point-defects and loop evolution.
Inert or Oxidizing anneal
Compute new loop distribution

Figure 3.6 Block schematic for model implementation in FLOOPS. The box in the middle represents the Ostwald ripening model described in Chapter II.

3.3.1 Modeling Loop Evolution from TEM Data

A model to predict the evolution of loops in an inert ambient was developed in Chapter II. Numerically calculated values of pressure are used in simulations for this work. Loop evolution is indirectly influenced by the presence of the loop ensemble, because of the pressure field it creates. The presence of a compressive field, for example, leads to an undersaturation of interstitials, thereby affecting the local concentration of point defects around the loops. Figure 3.7 illustrates the effect of a pressure field, from an ensemble of dislocation loops, on an impurity atom or point defect.

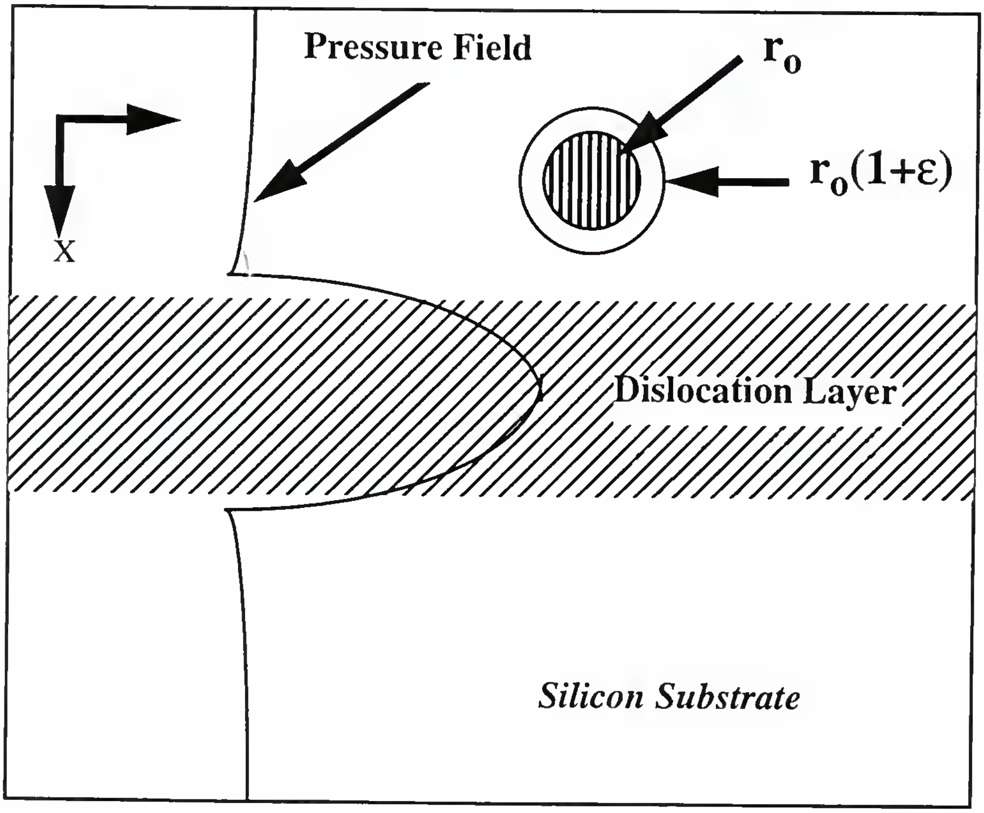


Figure 3.7 Interaction between the pressure field from a dislocation layer and a point defect in its vicinity; r_0 is the measure of the sphericity of the defect and ε is the dilatation which determines the elastic inclusion of the defect.

The interaction between the loops and the point defects described in the preceding paragraph is mathematically governed by the following equations:

$$C_I^*(P) = C_I^*(P=0)\exp\left(\frac{-P\Delta V_I}{kT}\right) \qquad 3\text{-}1$$

$$C_V^*(P) = C_V^*(P=0)\exp\left(\frac{P\Delta V_V}{kT}\right) \qquad 3\text{-}2$$

where $C_{I/V}^*(P)$ is concentration of interstitials in the presence of the pressure field, P is the spatially dependent magnitude of the pressure field, k is the Boltzman's constant, and T is the temperature. ΔV_I and ΔV_V are effective interstitial and vacancy expansion volumes, and are defined as

$$\Delta V_I = 1.33\pi\varepsilon r_o^3 \qquad 3\text{-}3$$

$$\Delta V_V = 2\pi r_s^2\gamma\Gamma/\mu \qquad 3\text{-}4$$

where r_o and ε are defined in Figure 3.7, r_s and Γ are the radius and surface tension of the vacancy well respectively, μ is the shear modulus of silicon, and γ is related to the Poisson's ratio η of the material (= 0.3 for silicon) as

$$\gamma = 3.0\cdot\frac{1-\eta}{1+\eta} \qquad 3\text{-}5$$

The value of ε used in the simulations is 0.5, which is reasonable in its meaningful range (0 < ε < 1).

3.3.2 Modeling the Strain from HRXRD Data

Park et al. [29] developed an analytical model for pressure from an ensemble of dislocation loops by summing the pressure contributions from individual loops. The model was limited to cases where the peak radius R_P was smaller than inter-loop distance L_{ALL}, i.e., the case in which the loops did not overlap. The simulation was also restricted by loop morphology and location. Pressure profiling in two-dimensions, for example under masked and unmasked regions, was not possible.

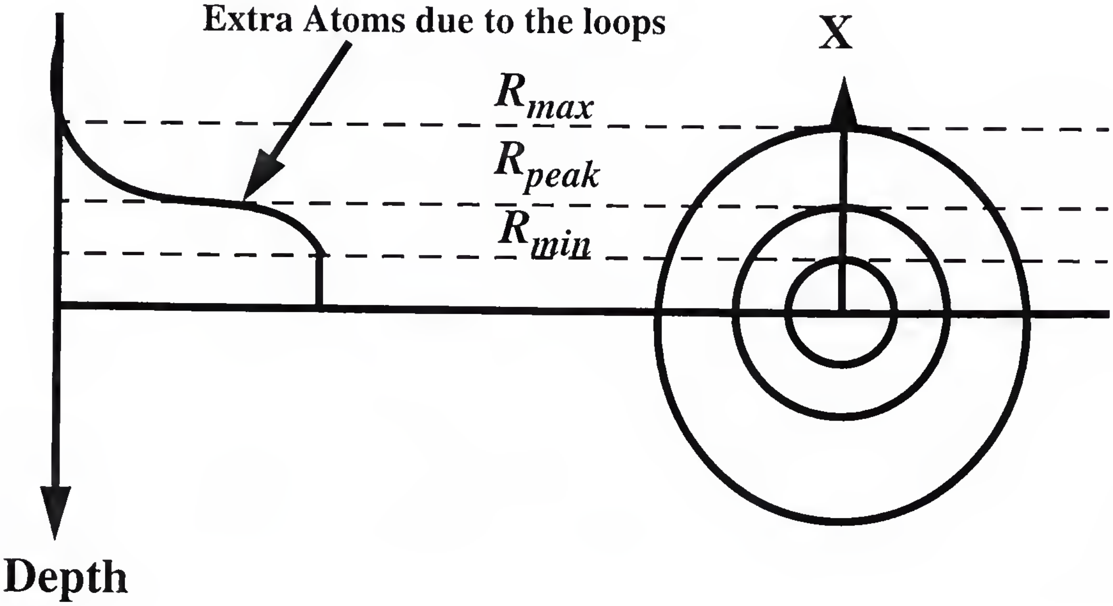


Figure 3.8 A plot of the extra number of atoms in the lattice due to the loops as a function of depth in the lattice.

A new numerical model based on the strain from the extra number of atoms in the lattice is developed in this section. It allows the loops to grow indefinitely till they overlap. It can be extended for simulating pressure from elliptical or other geometrically shaped loops. The two-dimensional extension of the model allows pressure values to be computed in masked and unmasked sections separately, and is the discussed as part of the next section.

The strain from an ensemble of dislocation loops can be thought of as the change in the lattice parameter the loops produce in the lattice. Thus, the number of extra atoms due to the loops should be a good indicator of the strain in the lattice. For a given dislocation-loop density this number increases as the core of the dislocation loop ensemble is approached, since more loops contribute to the number of extra atoms in the lattice. Thus, the peak strain in the lattice is expected to be near the core of the loops, as shown in Figure 3.8.

A mathematical expression for the plot in the Figure 3.8 is formulated as follows: the number of interstitials due to loops of radius R, and density $D(R)$, is given as

$$\pi R^2 \cdot D_{110} \cdot D(R) = 4 \cdot D_{110} \cdot D(R) \cdot \int_0^R \left(\sqrt{R^2 - X^2} \cdot dX \right) \qquad 3\text{-}6$$

where D_{110} is the density of silicon atoms in the <110> plane and X is the distance from the center of the loops as shown in Figure 3.8. If $N(X_R)$ is the depth dependent number of atoms due to loops of radius R, it follows:

$$\int_{-R}^{R} N(X_R)dX = 2\cdot\int_{0}^{R} N(X_R)dX = 4\cdot D_{110}\cdot D(R)\cdot\int_{0}^{R}\left(\sqrt{R^2-X^2}\cdot dX\right) \qquad 3\text{-}7$$

Thus the number of atoms trapped in the loops of radius R is

$$N(X_R) = 2\cdot D(R)\cdot D_{110}\cdot\sqrt{R^2-X^2} \qquad 3\text{-}8$$

which for all the loops is $N_{ALL}(X)$, given by

$$N_{ALL}(X) = \sum_{X}^{R_{max}} N(X) = 2\cdot D_{110}\cdot\int_{X}^{R_{max}} f_D(R)\cdot\sqrt{R^2-X^2}dX \qquad 3\text{-}9$$

Notice that the lower limit in the integral of Equation 3-9 is X because loops of radius less than X do not contribute atoms at that depth.

A finite element method is used to solve for the stress in the entire structure, using the quantity in Equation 3-9 to specify the normal component of the initial strain ε_0

$$\varepsilon_{XX0} = N_{ALL}(X)/5.02\times10^{22} \qquad 3\text{-}10$$

where the second quantity on the right hand side is the density of silicon atoms in the lattice. This can be converted to an initial strain force f_m for a volume V:

$$f_m = \int_V B^T \cdot D \cdot \varepsilon_0 dV \qquad 3\text{-}11$$

where D and B are the elasticity and strain-displacement matrix, respectively. This is used in the balance of forces equation described in Zienkiewicz and Taylor [44]. Nodal displacements are solved for and converted to stresses. The peak pressure in the structure is then obtained and divided by the bulk modulus, to obtain the peak strain. A plot of pressure in the lattice with increasing depth is drawn in Figure 3.9. The pressure peaks at the dislocation loop-core and decreases rapidly away from it.

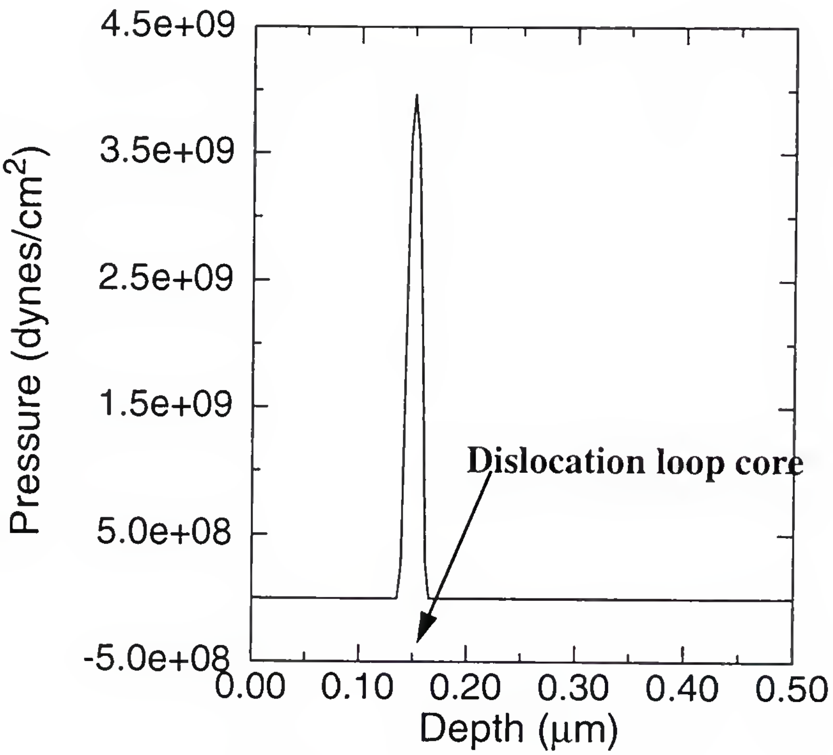


Figure 3.9 A plot of the simulated pressure in the substrate due to the loops. The compressive pressure peaks at the core of the dislocation loops. The absence of tensile stress at the edge of the loop layer is due to the displacement boundary condition used. This is further discussed in Section 3.3.3.

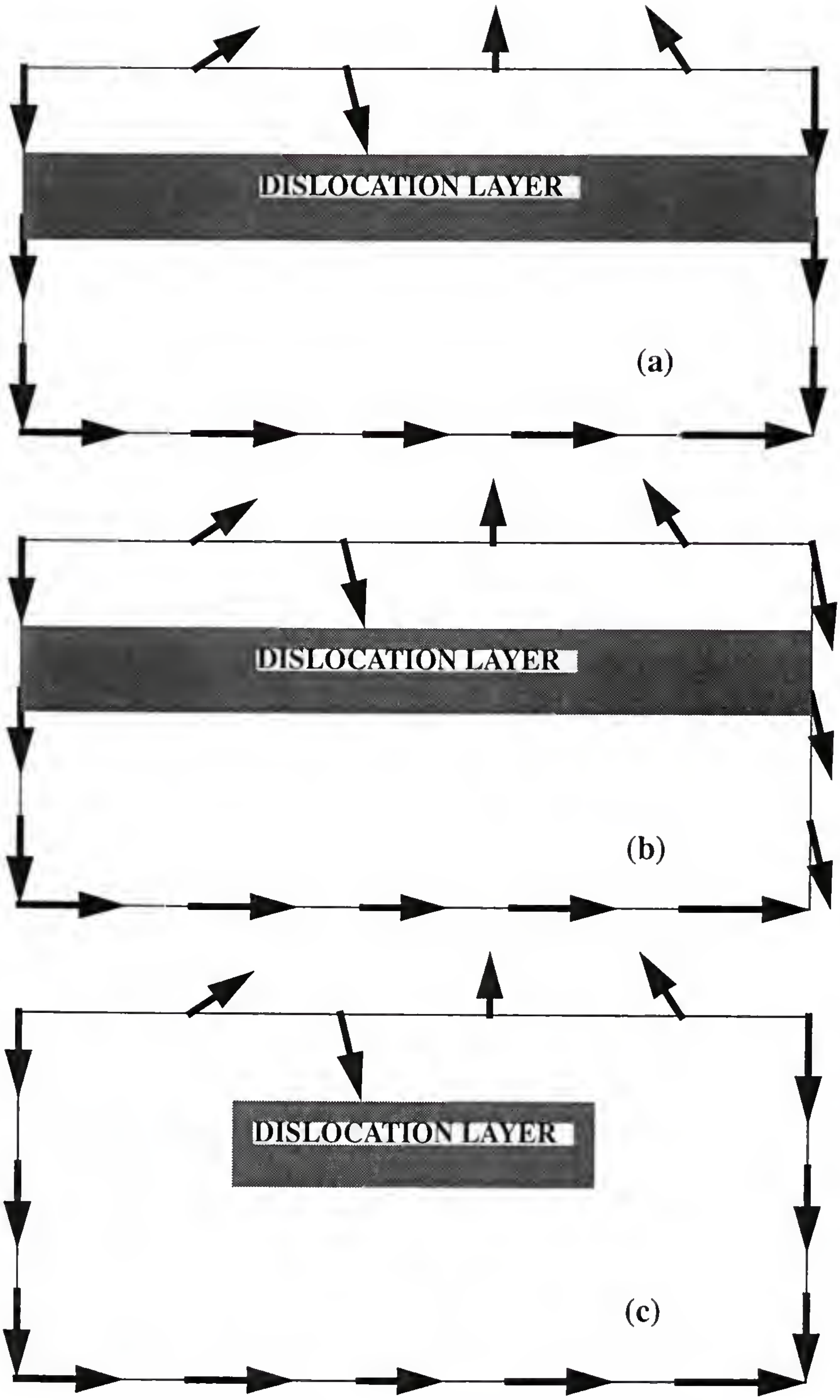


Figure 3.10 Boundary condition for normal displacement: (a) reflecting, (b) periodic, and (c) laterally restricted.

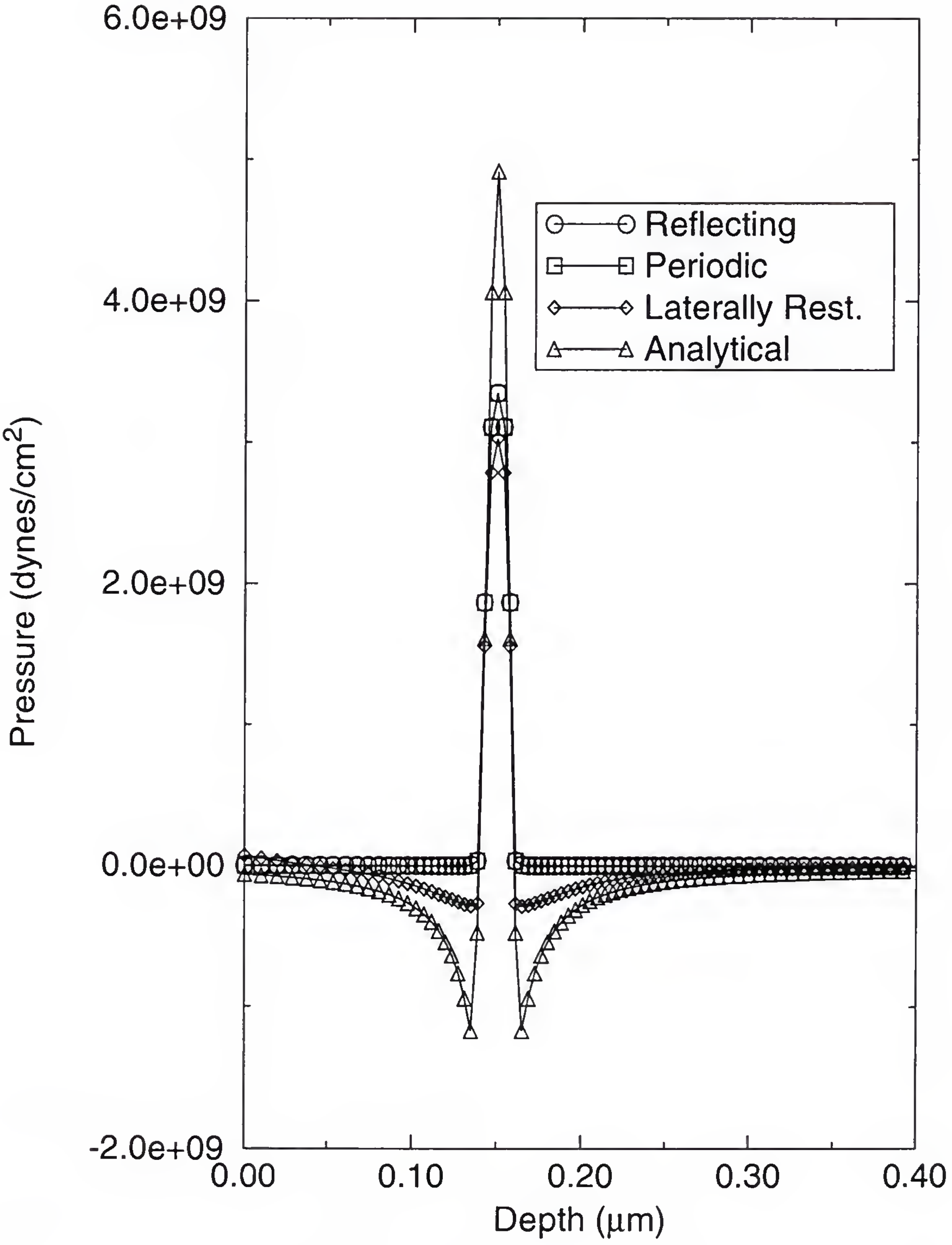


Figure 3.11 The effect of the lateral boundary conditions on the pressure around the dislocation loops. The effect of the boundary condition on the tension at the border of the loop layers is pronounced. However, the spread of the compressive pressure and its magnitude agree for all the boundary conditions studied.

3.3.3 The Effect of Boundary Condition

The magnitude of the tension at the loop boundaries is a strong function of the boundary conditions used in the simulations. The plot in Figure 3.9 is for a reflecting boundary condition where the normal component of the displacement is forced to be zero at the structure boundaries. This boundary condition is depicted in Figure 3.10 (a). The lateral edges, in this case, can be thought of as mirrors. The intended effect is to simulate the loops extending infinitely in both the lateral directions. Such a boundary condition is commonly used in mechanical and thermal problems to minimize the number of gird points, by simulating a unit cell of the periodic structure. The compressive pressure (Figure 3.11) predicted is close to the results from using the other boundary conditions. However, not allowing the lateral edges to move laterally forces the tension at the loop layer edges to be close to zero. The effect can be better understood by considering an elastic string that is pulled in one direction. It experiences a shrinkage in a direction perpendicular to the force. Likewise, the loops exert a compressive force in a direction perpendicular to the surface of the structure. This tends to push the lateral edges outwards. By preventing the edges from moving the boundary condition artificially induces a small compression which swamps out any tension existing at the loop boundaries. It is evident that to simulate this tension correctly some other approach is needed.

Cifeuntes and Stiffler [45, 46] used another approach to simulate periodic cells by using the “periodic” boundary condition. In this approach, depicted in Figure 3.10 (b), one of the lateral edges (the left one in this case), is used as the mirror, by forcing the normal component of the displacement to be zero along it. However, the other lateral edge is allowed to move by a constant distance. For the model implemented in FLOOPS, all the nodes along this edge are mapped on to the topmost node of the edge. Thus, all the nodes along the right edge are restricted to the same value of the normal displacement. If the center of the structure now lies on the left edge, the simulation mimics an infinitely extending loop layer. The main advantage of this approach is that it allows motion along the right edge. Some tension at the loop boundaries is observed (Figure 3.11), though the magnitude is smaller than the case of "laterally restricted" boundary condition which is discussed in the next paragraph.

The last set of boundary conditions investigated is the "laterally restricted" case. Simulations for a single loop reveal that pressure from it reduces to insignificant magnitudes at distances greater than twice the minimum inter-loop distance defined in Equation 3-13. Thus, the validity of this boundary condition arises from the fact that dislocation loops far away (laterally) from the regions of interest do not influence the magnitude of pressure. The loops are initialized for a lateral distance y defined as

$$-2L_{ALL} < y < 2L_{ALL} \tag{3-12}$$

$$L_{ALL} = \sqrt{\frac{0.5}{D_{ALL}}} \tag{3-13}$$

where D_{ALL} is the total density of all the loops. The boundary condition is illustrated in Figure 3.10 (c); the width of the shaded dislocation region is defined by Equation 3-12. The displacement at the lateral edges of the loop layers is now free and enhanced tension is observed at the loop layer boundaries. However, the magnitude of this tensile pressure is less than the analytical solution of Park, Jones, and Law [29].

3.4 Data Analysis

An analysis of Figure 3.5 shows that the strain decreases with increase in temperature. For temperatures below 1000°C, the loop density, number of captured interstitials, and strain do not change much with increasing anneal times. The average loop radius increases with anneal time, and is consistent with earlier work [Chapter II, 47, 48]. This section correlates the characteristics of the loop ensemble with the peak strain.

3.4.1 Correlation of Peak Strain with Captured Interstitials

For the 700°C, 800°C and 900°C anneals, no pronounced variation in the number of captured interstitials with anneal time is observed (Figure 3.4). This is reflected in the strain plots of Figure 3.5. The simulated values of the captured interstitials are higher in most cases, implying that some interstitials are being lost to the lattice. The model does not account for the strain from these "lost" interstitials. Since the strain from a free interstitial is expected to be higher than from an interstitial in a loop, the simulated values of strain are lower than the experimental values. However, this difference is not large for most anneal conditions. It is plausible that the interstitials released by the loops quickly diffuse away from the regions of high strain. Not accounting for the strain from them does not effect the accuracy of the simulations. For 1000°C anneal, the loops dissolve and the number of captured interstitials goes down rapidly. This causes the strain to fall sharply, and is seen in both the experimental and simulated data.

3.4.2 Correlation of Peak Strain with Loop Density and Radius

The loop density does not vary much at lower temperatures. However, at higher temperatures it begins to decrease with increase in anneal times. For the 800-900^{o}C temperature range the loop coarsening phenomenon is evident as the smaller loops dissolve and the larger loops grow. At higher temperatures, loops of all sizes dissolve, though their simultaneous coarsening is seen in Figure 3.3. The strain seems to have a similar trend, decreasing sharply at higher temperatures, and remaining almost flat for the lower temperature anneals.

Though it is clear that the loop radius increases with increasing anneal times, it is not readily apparent how the peak strain is related to the average loop radius. The average loop radius, which is an indicator of how large the loops are could be important in relating the spread of the strain in the lattice. The larger the loops, the larger the length of the strained lattice. Such information is available from simulations, but has not been verified by any experimental data (Figure 3.9).

3.5 Pressure Profiling for Two-Dimensional Structures

Section 2.4 discussed the implementation of a two-dimensional model for dislocation loop evolution. Simulations revealed the growth rate under the growing oxide was much larger than under the inert nitride due to the presence of the oxide injected interstitials. As part of a purely simulation effort, the effect of loop growth on the resultant pressure profiles is studied. It is assumed that the effect of the growing oxide on the substrate below is limited to the injection of interstitials and stress effects from it (which can be substantial for non-planar oxidation) are negligible.

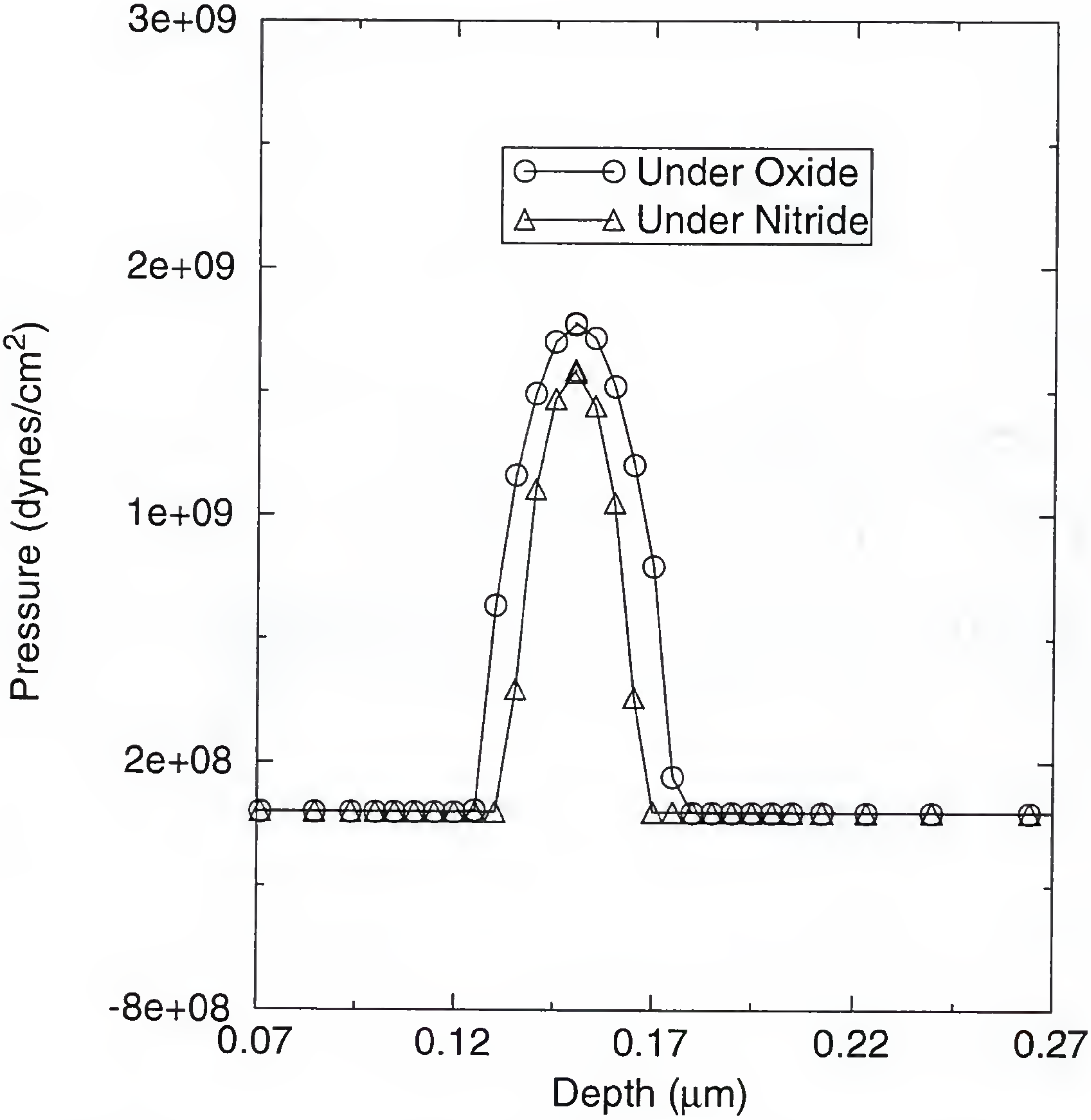


Figure 3.12 Pressure plots for dislocation loops annealed under an oxide and nitride for 60 minutes. The peak compressive pressure, and the spread, are larger for the loops growing under the oxide, where the injected interstitials contribute to faster loop growth.

As seen in Figure 3.12, the compressive pressure for the larger loops under the oxide is greater. The spread of this compressive pressure is also larger for the loops grown under the oxide. The reflecting boundary condition is used for the simulations.

3.6 Summary

A two-dimensional finite element model for strain from trapped interstitials is developed. Loop evolution is modeled using the Ostwald ripening phenomenon. Strain from free interstitials is not modeled in the study, and could account for differences in the simulated and measured values of strain. The model correctly predicts loop evolution in the inert ambient. The model underestimates the strain for long anneals in the 800-900°C range. Coupling of the strain to the local point defect concentrations is also implemented. Though not verified by experimental data, the pressure distribution in the lattice due to the loops is simulated.

CHAPTER IV
STRESS FROM THIN FILMS IN IC PROCESSING

Modern integrated circuit processing relies on the use of thin films for a myriad of purposes. Polysilicon films are used for contacts and short interconnects. Silicon dioxide films are either thermally grown (gate oxides in MOSFETS), or deposited by various Chemical Vapor Deposition (CVD) techniques. The latter category of oxides are frequently used as dielectrics between the various levels of metallization. Silicon nitride films are also frequently used in silicon processing. The self-limited thermal growth of these films leads to a reproducible process, since variables such as growth pressure, temperature, and time have a weak influence on the eventual film thickness. An important use of nitride films is as oxidation resistant masks in device isolation schemes, where oxides are selectively grown on recessed/semi-recessed substrates.Their high density enables nitrides to be frequently used as diffusion masks, in preference to silicon dioxide or silicon oxynitride films. On account of their high dielectric constants, nitrides are also used as dielectric barriers in silicon technology. Epitaxial layers have become very common in modern technology. In MOSFETs they are used to improve the latchup resistance. They are also useful in reducing alpha-particle induced soft errors in memory devices.

The use of thin films in silicon technology is accompanied by stress in the thin films themselves and in the silicon substrate below. Films like silicon nitride, CVD oxide, etc., have elastic stress present in them as an inherent part of the deposition process. This stress can either be tensile or compressive, the sign and magnitude being strongly dependent on the processing parameters, viz., substrate temperature, type of substrate, rate and method of deposition. The sign of the stress in the film can easily be determined by looking at the shape of the film-substrate composite structure, as illustrated in Figure 4.1. A convex curvature results when the relaxed film is forced to fit (compressed) onto a substrate of shorter length (Figure 4.1 (a)). In this case the film is in compression, while the substrate immediately below it is in tension. However, if the film needs to be stretched to fit on the substrate, it experiences a tensile force, and the substrate below it is in compression (Figure 4.1 (b)).

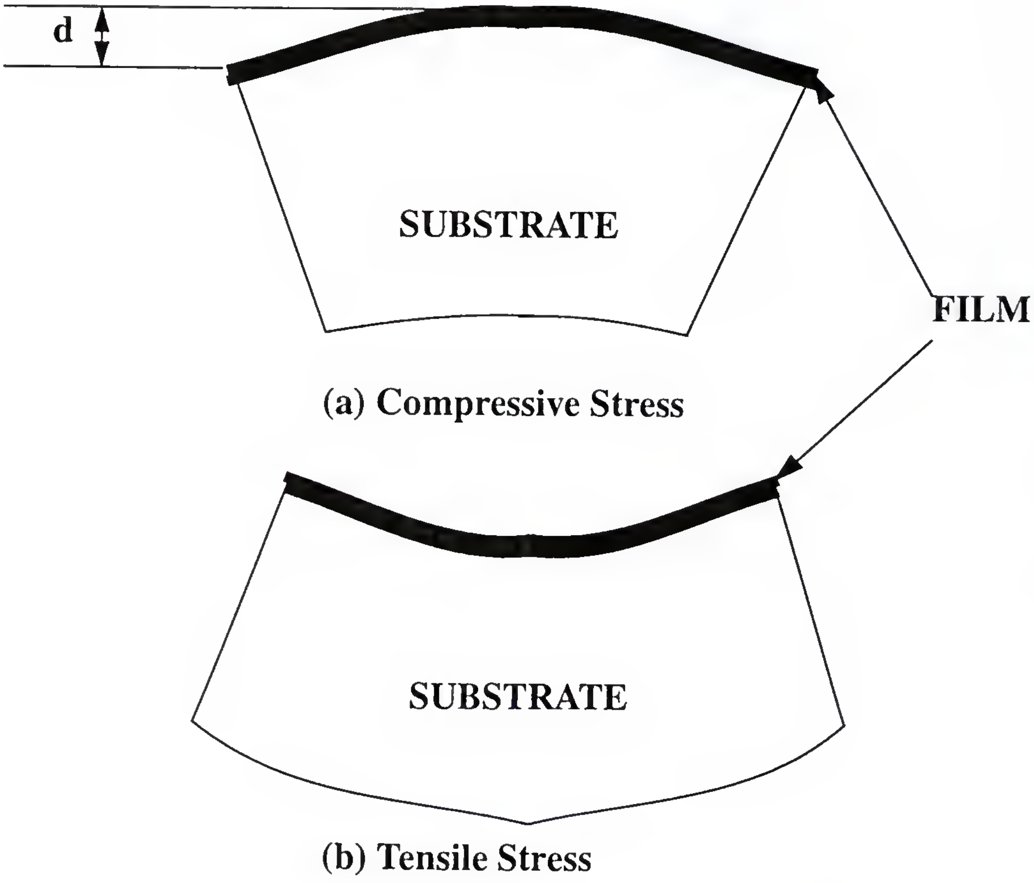


Figure 4.1 Thin film stress; (a) convex curvature indicates a compressive stress in the film, while (b) concave curvature represents a tensile stress in the film.

Thin film stress can be subdivided into two major components. The thermal component σ_{th} arises due to the difference in the thermal expansion components of the film and the substrate, and is given as

$$\sigma_{th} = Y_F(\alpha_F - \alpha_S)\Delta T \qquad 4\text{-}1$$

where Y_F is the Young's modulus of the film, α_F and α_S are the thermal expansion coefficients of the film and substrate, respectively, and ΔT is the film deposition or growth temperature minus the temperature at which the stress is measured. The intrinsic stress of the film is more complex and less understood. It is a strong function of film deposition conditions such as temperature, pressure, and gas flow rates. Changes in film deposition parameters may change the magnitude or even the sign of the resultant stress in the film.

A convenient way to analytically calculate the stress in a thin film is to measure the magnitude of wafer bending (d in Figure 4.1 (a)) caused by the deposition or growth of the film. If Y_S and Y_F are the Young's modulus of the silicon substrate and film, respectively, t_S and t_F the thickness of the substrate and film, respectively, L is the length of the substrate, and μ is its Poisson's ratio, the film stress is given from plate bending theory [49] as

$$\sigma_F = \frac{dY_S t_S^2}{3L^2 t_F(1-\mu)} \cdot \left(1 + \frac{Y_F}{Y_S} \cdot \frac{t_F}{t_s}\right) \qquad 4\text{-}2$$

which for a very thin film reduces to

$$\sigma_F = \frac{Y_S t_S^2}{6rt_F(1-\mu)} \qquad 4\text{-}3$$

where r $(=L^2/2d)$, is the curvature of the bent substrate.

High values of stress from thin films can detrimentally affect the operation of devices. For example, a compressive stress in the substrate can retard the diffusion of boron [50, 51]. If the film is not continuous or is non-planar significant stress is generated in the substrate [52, 53], which might then yield to form dislocations. Analytical models like those given in Equations 4-2 and 4-3 suffice for simpler geometry. For complex shapes frequently encountered in modern device processing, a more robust technique with a correct set of boundary conditions is needed. This chapter attempts to model stress effects in silicon due to nitride stripes and epitaxial growth. The finite element code in FLOOPS is used to numerically simulate stress in the silicon substrate. The use of proper boundary conditions to simulate periodic structures commonly found in ULSI technology is investigated.

4.1 Stress from Nitride Stripes

Nitrides are often patterned on the silicon substrates as isolation masks or as diffusion barriers. For structures like memory circuits equidistant nitride stripes are patterned on the silicon substrate. If these stripes are very wide, the stress in the substrate is not very pronounced and does not affect the device operation. However, if the stripes are narrow, high levels of stress are generated around the nitride mask edges.

4.1.1 Implementation in Finite Element Code

The finite element code is a robust method to calculate stress from a variety of sources. The finite element code in FLOOPS is used to simulate the effect of intrinsic stress in nitride films on the substrate, by specifying the lateral component of the initial strain ε_{YY0}. This can be converted to an initial strain force f_m for a volume V in the nitride as

$$f_m = \int_V B^T \cdot D \cdot \varepsilon_0 dV \qquad 4\text{-}4$$

where D and B are the elasticity and strain-displacement matrix respectively. This is used in solving the balance of forces equation [44]. Nodal displacements are solved for and converted to stresses. The viscoelastic code in FLOOPS is used in its elastic limit by specifying a large (~$1\text{x}10^{20}$ Po.) number for the viscosity for both the nitride and silicon.

4.1.2 A Single Nitride Stripe

Figure 4.2 illustrates the displacement vectors due to a single nitride stripe, 5 microns wide and 200 Å thick. The lateral edges are not constrained and are free to move vertically. The substrate is 5 μm thick and its bottom edge is constrained from moving downwards; though lateral motion is allowed. This set of boundary conditions corresponds to an isolated nitride stripe-silicon substrate composite structure. The displacement vectors in the plot can now be analyzed from first order physics. The deposited nitride is assumed to be under tension. If the stripe extends over the entire substrate, a compressive stress, 2~3 orders of magnitude less than in the nitride would exist in the substrate below. This is because the substrate is 2~3 orders of magnitude thicker than the nitride. However, if the nitride is patterned, as is the case for the simulation in discussion, the edge effects cause a large stress to be generated in regions close to the edge. The tension in the nitride causes a "lift-off" effect in the region to the left, causing it to go into tension. The region immediately below the nitride is pushed down and is in compression. A pressure plot from left to right illustrating this above behavior is illustrated in Figure 4.3.

4.1.3 Stress from Multiple Nitride Stripes

Periodic structures consisting of identical unit cells are common to many semiconductor devices like memory chips. Thus, a pattern of nitride stripes of equal width and spacing are commonly found during ULSI processing. If the stripes are sufficiently close to each other, as is the case for scaled devices, the isolated behavior discussed in the previous section ceases to be valid. Stress from neighboring stripes can effect the local pressure values. This section looks at the effect of multiple nitride stripes on the net pressure in the substrate below. A large number of stripes are initially simulated and then their number reduced till there is no loss of accuracy. It was observed that a minimum of three stripes are necessary to mimic the periodicity of the entire structure.

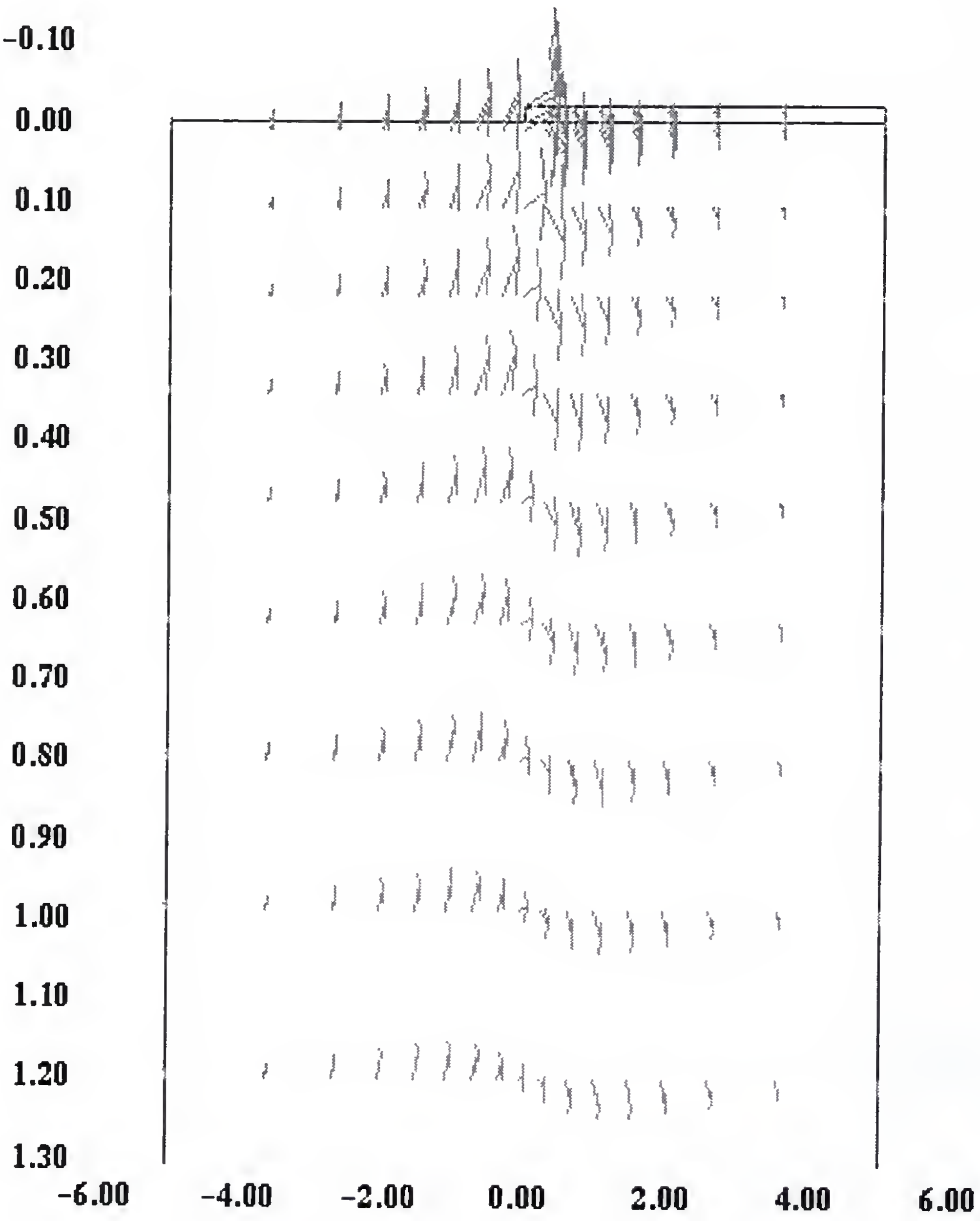


Figure 4.2 Displacement vectors due to intrinsic stress in a single nitride stripe. The lateral edges are allowed to move vertically. The tensile stress in the nitride tends to pull the silicon substrate up at the left side (in tension), and push down the region immediately below it (in compression), as is seen by the displacement vectors. A plot for the actual stress in the substrate is shown in Figure 4.3.

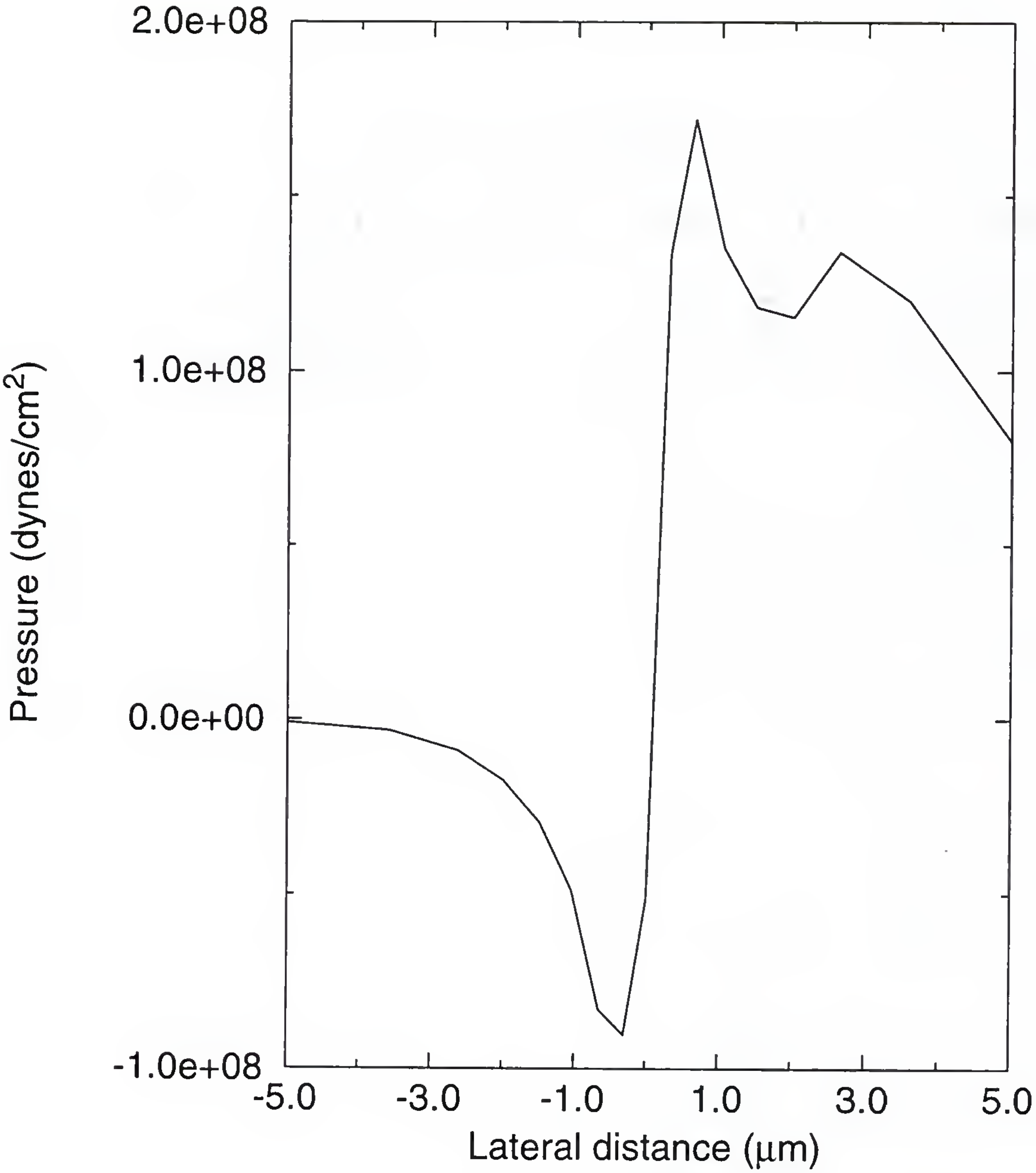


Figure 4.3 Pressure plot for a lateral cut (x=0.2 microns) through the structure shown in Figure 4.2. The stress changes from tension to compression from left (bare) to right (covered with nitride). The intrinsic tension in the nitride film is 1.4e10 dynes/cm^2.

The structure in Figure 4.4 shows multiple nitride stripes, 5 microns wide and apart, and 200 Å thick, patterned on the silicon substrate. The effect of the neighboring stripe on the local values of stress is evident from the plot. The tension at the left edge of a single cell is enhanced, while under the nitride the compressive forces are reduced. This is to be expected, as the adjacent stripes on both the left and right of the unit cell add to the tension, increasing the tensile forces on the left and decreasing the compressive forces below the nitride. The stress in the silicon substrate is a strong function of the stripe thickness and width. This dependence is discussed throughout this chapter.

The principle slip pattern in silicon for the <111> plane is the <110> direction. This corresponds to the force due to the shear stress component. A value of 3×10^7 dynes/cm^2 has been reported by Hu [12] to be the critical shear stress for slip in silicon. Dislocations in regions having a shear stress component greater than this value will move. The shear stress contours for the nitride stripes under discussion are shown in Figure 4.5. The contour is a double lobe because the shear stress is related to the polar coordinates as

$$\sigma_Z = (\sigma_r - \sigma_\theta)\sin 2\theta + \sigma_{r\theta}\cos 2\theta \cong \sigma_r \sin 2\theta \qquad \text{4-5}$$

the function $\sin 2\theta$ peaking at 45 degrees from the vertical edge. The plot indicates that a dislocation moving under the influence of the stress field will continue to do so till it passes under the mask edge, where it might get stranded as the shear stress value may fall below the critical value for slip. The plot also shows that the nitride film's influence, as regards the shear component, extends about 1 micron deep and ± 2 horizontally from the edge. This could be significant in scaled ULSI structures. A behavior similar to this was presented in Figure 1.6.

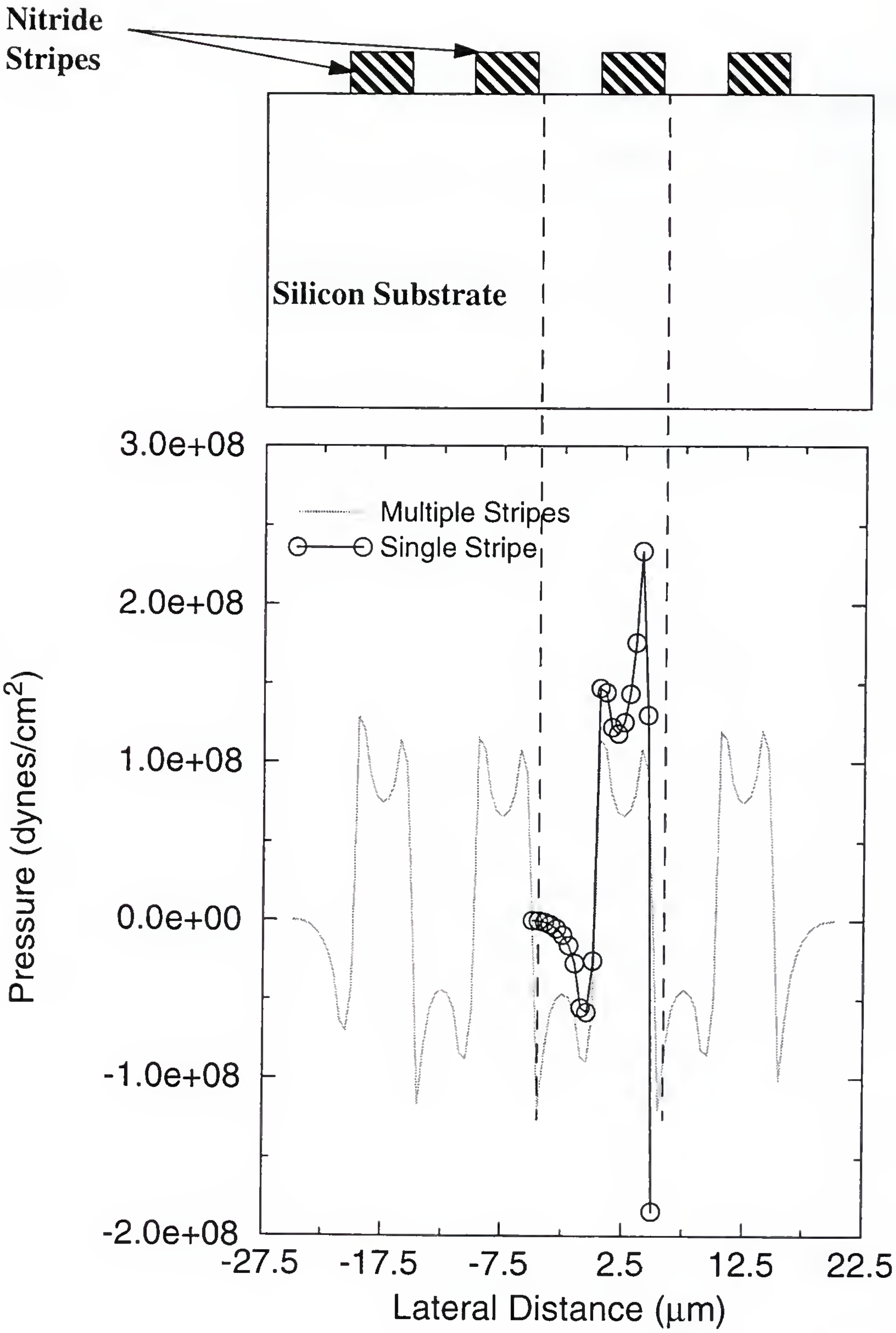


Figure 4.4 Multiple nitride stripes used to simulate pressure contours. The plot depicts the effect of neighboring stripes on the local stress.

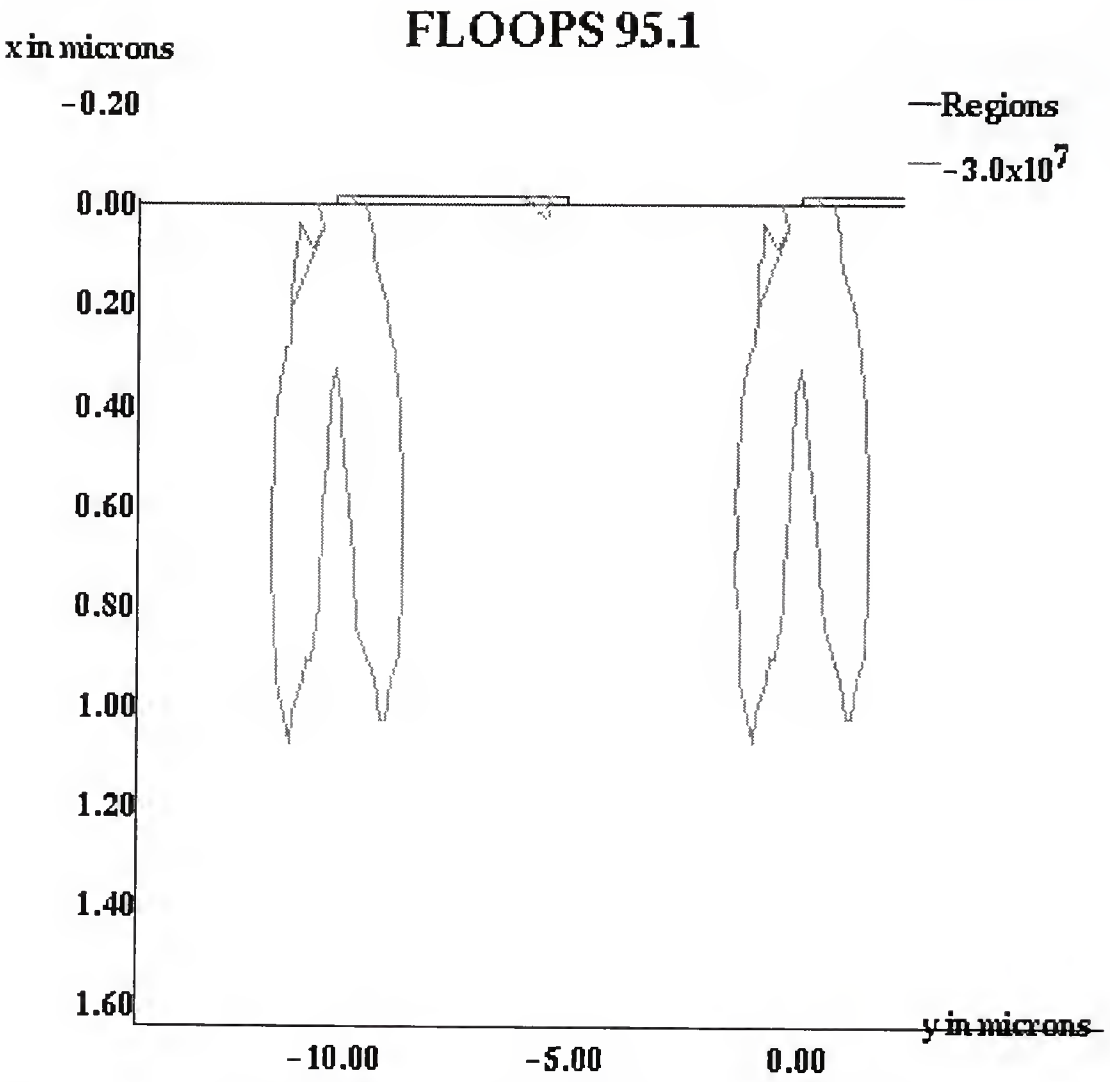


Figure 4.5 Shear stress contours (for -3×10^7dynes/cm^2) due to intrinsic stress in a deposited nitride stripe. The lobes peak at 45 degrees and represent critical values for dislocation loop glide.

4.1.4 Stripe Width Dependence of Stress from Multiple Stripes

As the nitride stripes are made smaller and brought closer together a greater interaction between them is expected. The hydrostatic component of the stress (i.e. pressure), as well as the shear component follow the laws of algebraic superposition, where the stress at a point is the linear sum of the stress from all the stripes in the structure. A plot of the pressure for different nitride stripe widths is shown in Figure 4.6. The thickness of the nitride film is kept constant at 0.1 μm in the simulations. In the regions immediately below the film/substrate interface an increase in the peak values of both the compression and tension is observed with decreasing stripe width and spacing. The compressive pressure peak due to the 2.5 μm stripe is almost three times that of the 10 μm stripe and the trend would continue for smaller stripe widths.

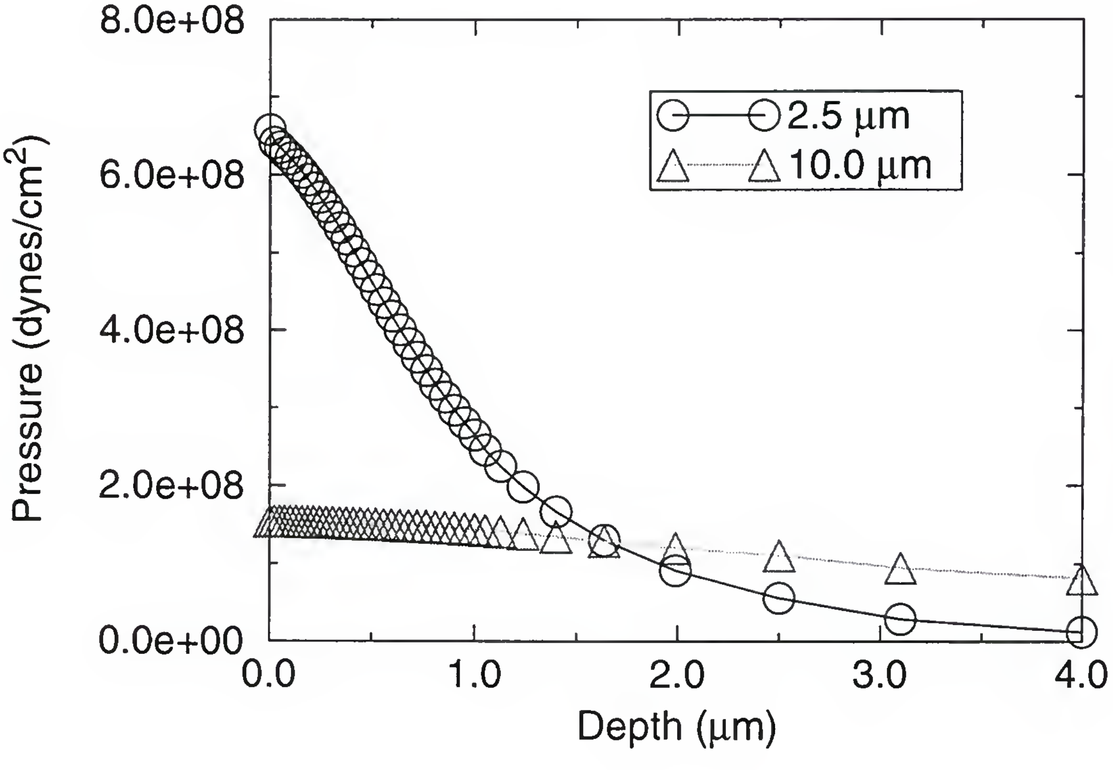


Figure 4.6 Plots of pressure, as a function of depth in the silicon substrate, in the middle of the stripe, for various stripe widths, and a nitride film thickness of 0.1 μm. As the stripes get smaller and closer, the compressive and tensile pressure peaks get bigger in magnitude, indicating the effect of the neighboring stripes. However deeper in the substrate stress from the wider stripes is higher.

A completely different scenario exists if we look at the stress levels deeper in the substrate. At roughly about 1.5 microns the stress from the 10 μm stripes becomes greater than the 1 μm wide stripes. This is because stress due to the smaller stripes falls off rapidly, while it extends deeper into the substrate for the wider stripes.

4.1.5 Shear Stress in Substrate from Multiple Nitride Stripes

The effect of multiple nitride stripes on the shear component of the stress is markedly different. This section examines the stripe width and thickness dependence of the shear stress in the silicon substrate.

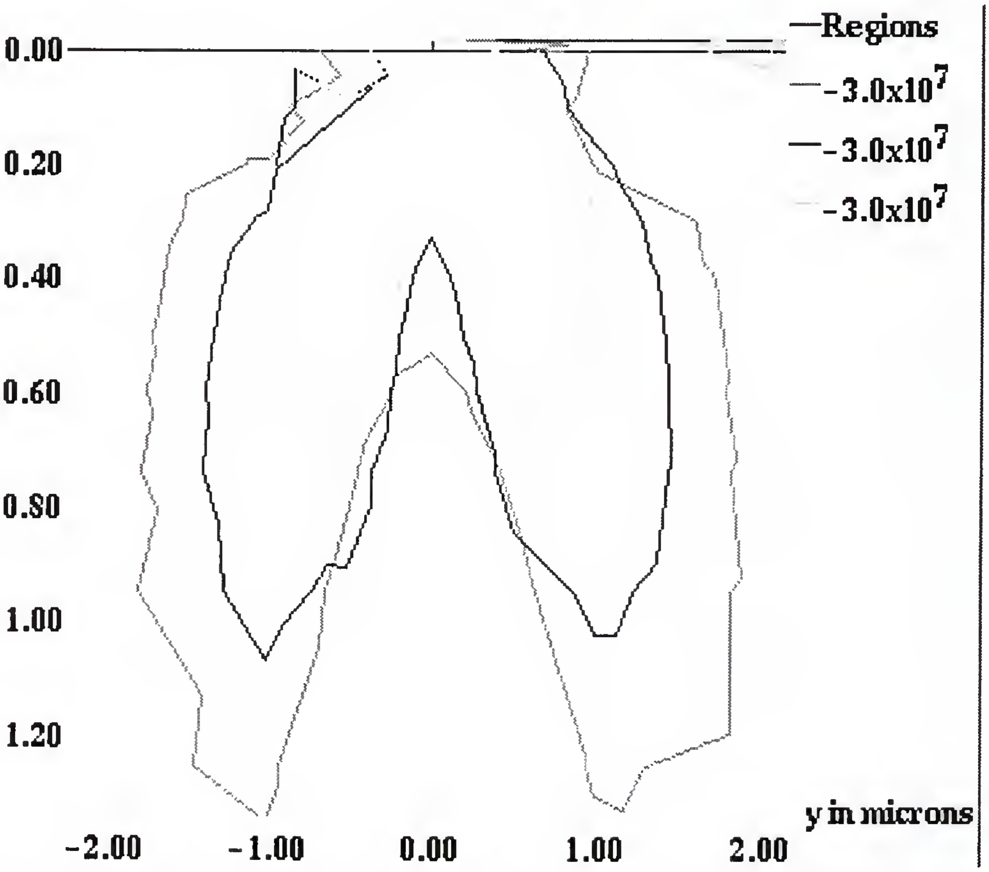


Figure 4.7 Shear stress contours for the critical value of dislocation glide (~$3x10^7$dynes/cm^2) for varying stripe widths.

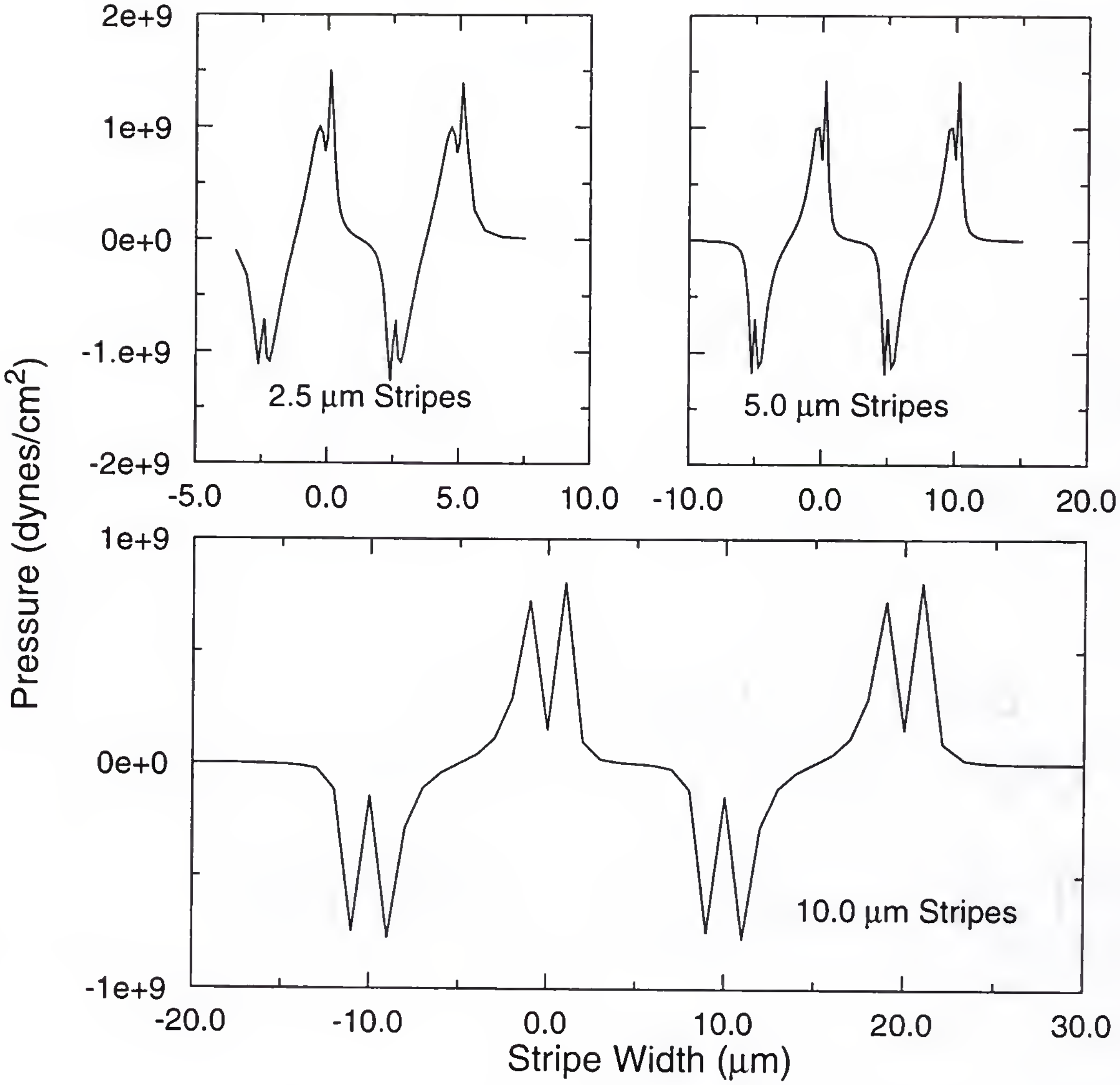


Figure 4.8 Lateral variation in shear stress, at a depth of 0.1 μm for varying stripe widths for a 0.2 μm thick nitride stripe. The peaks at the edges of the stripe begin to overlap as the stripes are brought closer together.

As the stripes are bought closer together, the shear stress components tend to offset each other; the tensile component from the one stripe offsets the compressive component of the adjacent stripe. The effect is illustrated, for decreasing stripe widths, in Figure 4.7. The lobes for the 2.5 μm stripe are the smallest, and the region of dislocation glide is roughly half that of the 10 μm stripes. Thus, as the stripes are brought closer together, the hydrostatic component of stress add up while the shear components offset one another in regions immediately below the nitride-silicon interface.

The contours in Figure 4.7 indicate that the shear stress peaks near the edge of the patterned film. Since the shear component of stress has implications on bulk processing (e.g. dislocation loop glide and substrate yielding), it is useful to investigate its lateral variation under the patterned film. Results of the simulations are plotted in Figure 4.8 for a 0.2 μm thick nitride stripe. The stripe widths range from 2.5 μm to 10 μm. The plots are at a depth of 0.1 μm below the nitride silicon interface. For the case of the widest stripes the shear stress "peaks" are smaller in magnitude and reduce to almost zero in the middle of the stripe. However, as the stripes are made smaller and brought closer together the peaks begin to overlap in the middle of the stripes.

4.1.6 Film Thickness Dependence of Stress from Multiple Stripes

The use of a nitride layer as a diffusion or oxidizing mask is often limited by its thickness. It would be interesting to look at the effect of nitride stripe thickness on the stress in the substrate below. A first order analysis makes it obvious that a thicker nitride would result in larger numbers for stress in the substrate below. The simulations not only reveal results in accordance with this analysis, but also suggest that the ratio of the film thickness to its width is important in determining the shape of the pressure plot in the substrate immediately below the middle of the stripe.

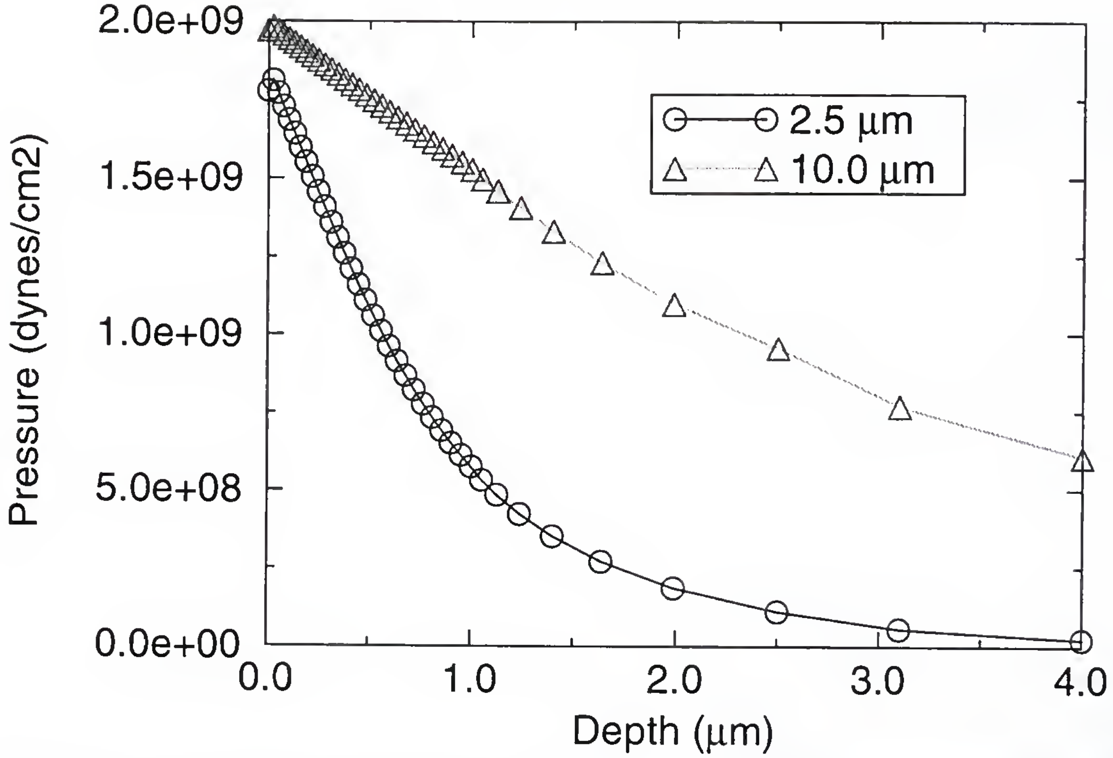


Figure 4.9 Pressure plots in the middle of the stripe for various stripe widths for a nitride film thickness of 2 µm. As the stripes get smaller and closer (in contrast to Figure 4.6), the compressive pressure gets smaller in magnitude.

The "stripe width" dependent behavior discussed in section 4.1.4 remains valid as long as the thickness of the nitride film is small compared to its width. However, if the thickness of the film is increased and becomes comparable with the width of the stripe, the "stripe width" dependence of the stress in the substrate below markedly changes. The average hydrostatic pressure (stress) now decreases with shrinking stripe width, in contrast to the results of the previous section (Figure 4.9). The simulation is for is for a 2µm thick nitride stripe for stripe widths ranging from 2.5 to 10 µm. The pressure due to the wider (10 µm) stripe is now larger, when compared to the smaller (2.5 µm) stripe. As in the case of the thinner film, the stress from the wider film extends deeper into the substrate, while it falls rapidly for the smaller stripe.

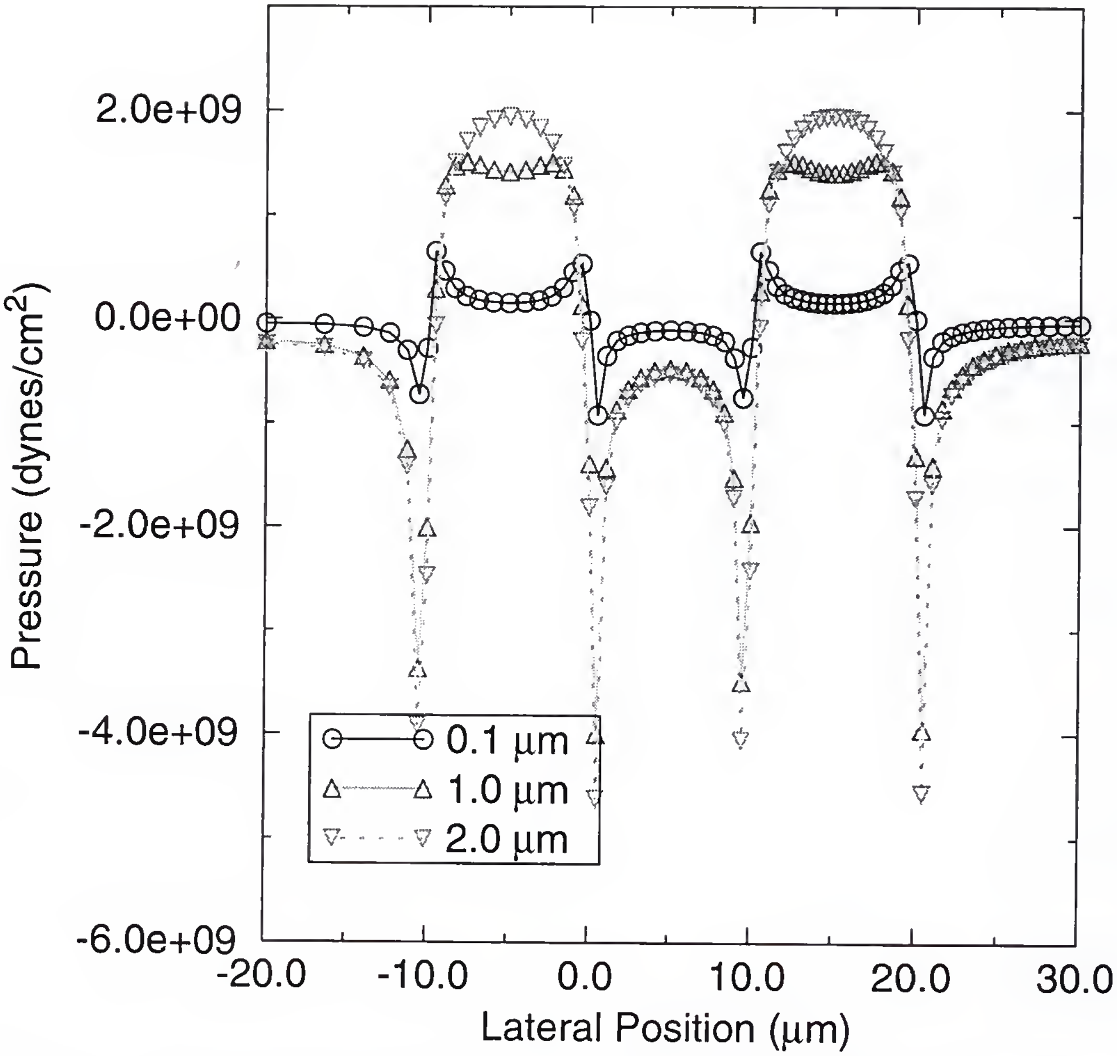


Figure 4.10 Film thickness dependence of the pressure in the silicon substrate for the case of 10 µm wide stripes at a depth of 0.1 µm. The pressure increases as the thickness of the film is increased. Also, the shape of the plot changes from convex to concave at a thickness of approximately 1.25 µm.

It is also interesting to observe the effect of increasing film thickness on the lateral variation in the hydrostatic pressure. A look at Figure 4.10 indicates that the shape of the pressure plot in the middle of the stripe is convex for very thin films. However, if the film thickness is increased ten fold to 1 µm, the pressure variation in the middle of the stripe changes from convex to an almost flat shape. If the thickness of the film is further increased to 2 μm, the pressure variation is concave, i.e., the compressive pressure is maximum in the middle of the stripe. Therefore, the ratio of the width to the thickness (w/t) is important in determining the shape and magnitude of the stress in the substrate below. A quantity, $(w/t)_{crit}$, can be defined as the ratio of the width to the thickness of the nitride film for which the lateral variation in pressure in the region immediately below the middle of the deposited stripe is flat. For the 10 μm stripe width the critical ratio ($(w/t)_{crit}$) is found to be ~ 8.

As discussed earlier, the ratio of the width (w) of the stripe to its thickness (t) is critical in determining the lateral variation of the pressure. Simulations were performed to investigate the dependence of $(w/t)_{crit}$ as a function of the stripe width. The variation of the $(w/t)_{crit}$ is found to be perfectly linear with stripe width (Figure 4.11), corresponding to a slope of ~ 8. This ratio is valid for shallow depths in the substrate (< 0.4 μm). Since bulk processing is predominantly dependent on stresses in regions at this depth, this ratio assumes importance. It is valid for all stress levels in the film. If the compressive pressure immediately below the middle of the stripe is taken as the reference, films with

$$w/t > 8 \tag{4-6}$$

will show a decrease in the pressure with increasing stripe width, and films with

$$w/t < 8 \tag{4-7}$$

will show a increase in pressure with increasing stripe width.

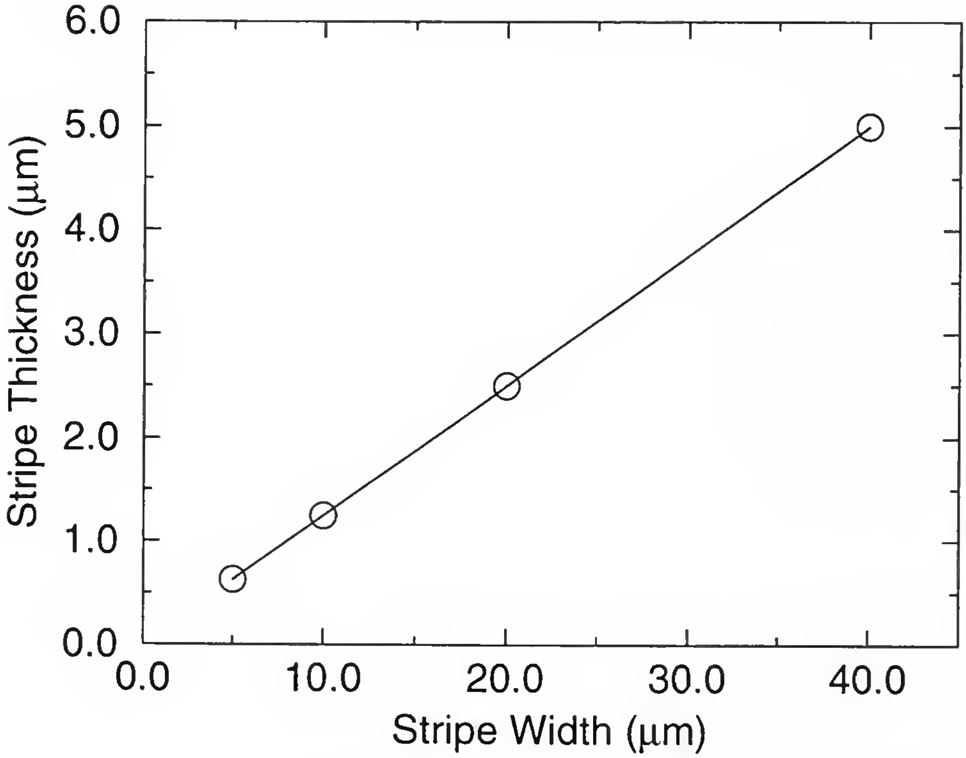


Figure 4.11 The variation of stripe thickness with stripe width, which results in a flat pressure profile in the middle of the stripe. The variation is found to linear with a slope of ~ 1/8.

4.1.7 Film Thickness Dependence of Shear Stress

Widely spaced stripes (10 microns) are chosen to investigate the effect of film thickness on shear stress. Figure 4.12 illustrates the effect of increasing nitride thickness on the shear stress component in the substrate below. The lobes are poorly formed for the 50 Å nitride. As the thickness of the nitride film is increased the characteristic twin lobes develop and the area of influence extends deeper and wider in the substrate. It is evident that an upper limit exists to the nitride thickness that can be used as a mask.

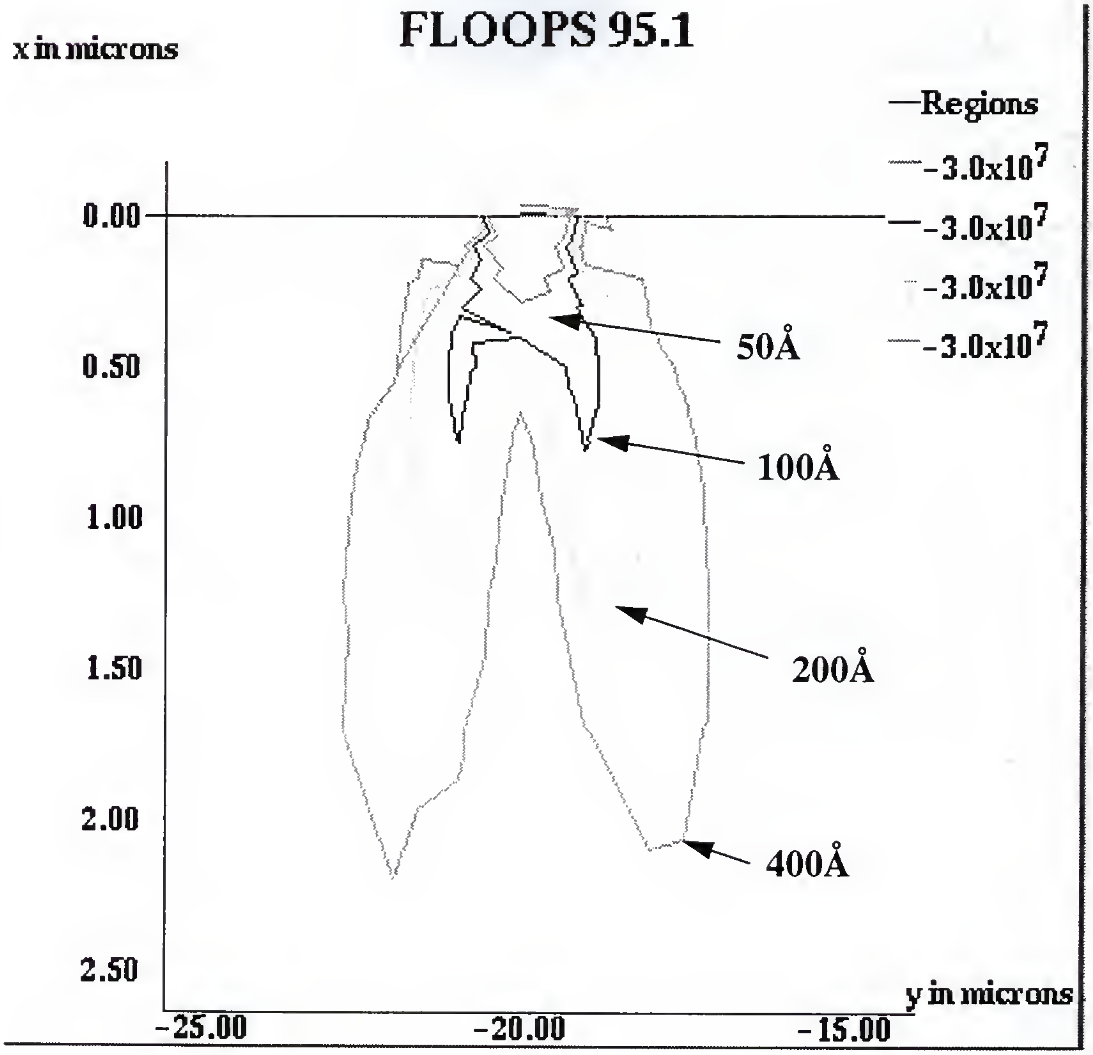


Figure 4.12 Shear stress contours for varying nitride thicknesses. The characteristic twin lobes barely begin to form for a 50Å thick nitride, but are well developed and much deeper for thicker nitrides. The jagged edges in some of contours are grid related and not a real effect.

4.2 Wafer Curvature Due to Lattice Mismatch

The use of epitaxial films, where single crystal silicon is grown on top of the silicon substrates, is a standard feature of many ULSI processes. Epitaxial p/p^+ structures are frequently used to improve latchup susceptibility in CMOS devices and to reduce the frequency of alpha-particle induced soft errors in memory devices. An artifact of the epitaxial process is the lattice mismatch that results from the difference in dopant concentrations in the substrate and the epitaxial layer. The heavily doped side, i.e. the substrate, is relaxed from the melt process. However, the growth of the lightly doped epitaxial layer causes an interfacial mismatch of the lattice parameter. This mismatch is directly proportional to the difference in the dopant concentrations.

Depending on the level of the mismatch the epitaxial-substrate composite reacts in two ways. If the mismatch is below a critical value, the system relaxes by bending the substrate. If the strain due to the mismatch exceeds the yield value of the system, misfit dislocations are generated. Wafer bending is not desirable from the lithographic standpoint and misfit dislocations may affect the yield of the process.

Lin et al. [26] investigated the effect of lattice mismatch on wafer bow. They reported the wafer bow was directly proportional to the level of the interfacial doping mismatch and the thickness of the epitaxial layer. They also reported the successful use of a technique called "compensation," which reduced the magnitude of this interfacial mismatch.

This section develops models for wafer bow and the resultant stress in the silicon substrate and the epitaxial layer. It is assumed that the epi-substrate composite has not yielded to form dislocations. However, stress levels predicted by the simulations could be used to predict the regions along the epi-substrate interface where dislocation are most likely to form. Additionally, the technique of "compensation" is simulated and the model is verified from the data in Lin et al. [26].

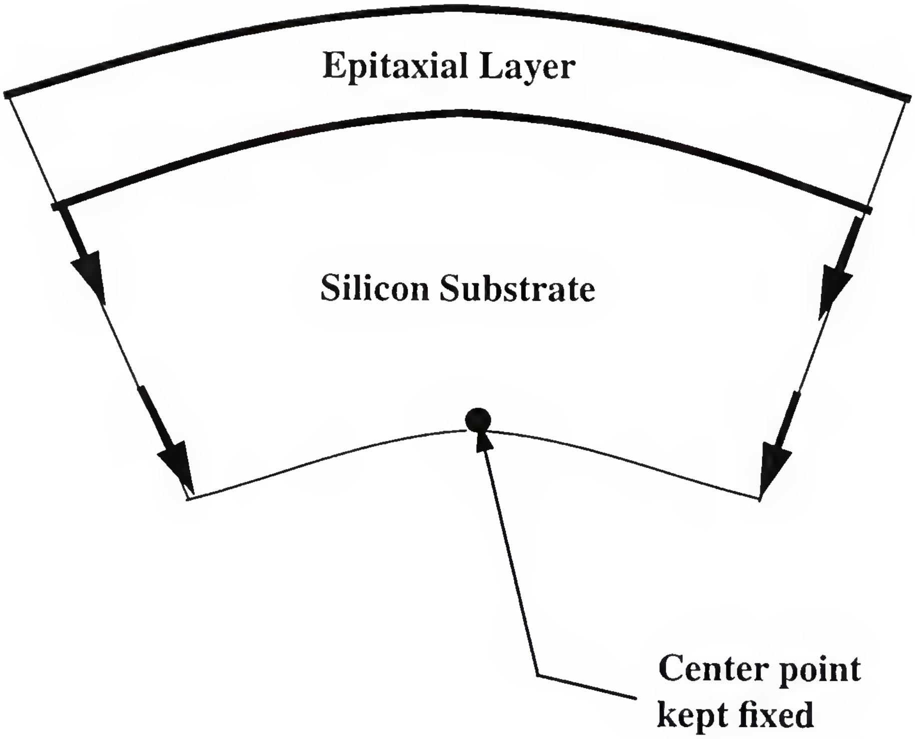


Figure 4.13 Diagram illustrating the boundary condition for displacement in the finite element code used to simulate wafer curvature due to the lattice mismatch between a heavily doped substrate and a lightly doped epitaxial layers.

It is well known that doping with boron causes the silicon substrate to contract (~ 0.014 Å/at. % boron). A relation between the substrate boron doping C_B and the initial lateral strain ε_{YY0} that results in the epitaxial layer is given as

$$\varepsilon_{YY0} = -\frac{0.014}{L_S} \times \frac{C_B}{5\times10^{22}} \times 100 \qquad 4\text{-}8$$

where L_S is the lattice constant of undoped silicon. This is converted to an initial strain force for the finite element code by Equation 4-4. The boundary condition used for the analysis is depicted in Figure 4.13. The lateral edges are left free to move either vertically downwards and/or laterally sideways. The bottom edge of the structure is also left free with the exception of one point at the center, which is kept fixed to prevent rigid body motion. The entire wafer is then simulated and the displacement at the lateral edges are a direct measure of the wafer bow.

Figure 4.14 depicts the magnitude of the wafer bow for a lightly doped epitaxial layer and a heavily doped substrate ($2x10^{19}/cm^3$). This results in an interfacial lattice mismatch of about $5.6x10^{-4}$ Å. As the thickness of the epitaxial layer is increased the wafer bow increases.

Figure 4.15 (a) depicts the wafer bow as a function of the interfacial mismatch, represented as a net strain. The mismatch between the substrate and the epi layer can be reduced by means of a technique called “compensation” [26]. In this technique the substrate is grown out of a melt consisting of germanium, which acts to increase the lattice constant of silicon. This compensates the contraction caused by presence of the boron. For a germanium to boron ratio of 8, complete lattice compensation is measured in the lattice. This corresponds to the zero strain data point in Figure 4.15 (a). Figure 4.15 (b) depicts the effect of increasing the epitaxial thickness on the resultant wafer bow, for a constant mismatch between the epi layer and the silicon substrate.

As shown by the displacement plots in Figure 4.14, the wafer curvature increases with increasing epi layer thickness, because the thicker epi layer exerts a large stress on the substrate. If the yield stress of silicon is exceeded then structure will deform by forming interfacial dislocations. Thus, the boron doping in the substrate and the thickness of the epitaxial layer are limiting factors for dislocation free structures. The use of germanium to compensate the lattice alleviates this problem to some extent. Lin et al. [26] showed improvement in hold times for memory devices fabricated using the germanium compensation method.

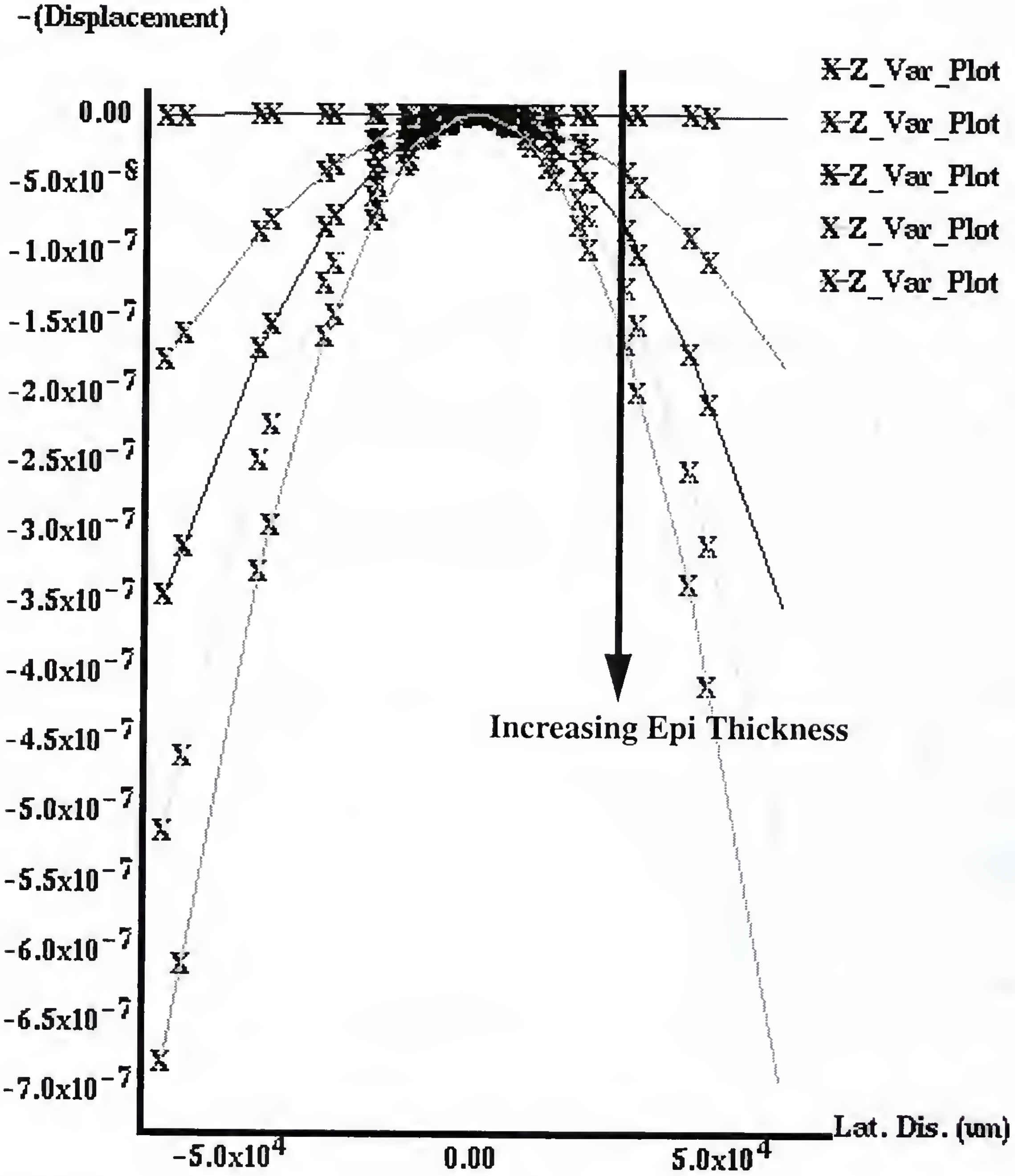


Figure 4.14 Displacement plots depicting the extent of the wafer bow for a substrate boron doping of $2\times10^{19}/cm^3$. The wafer bow increases with increasing epitaxial thickness.

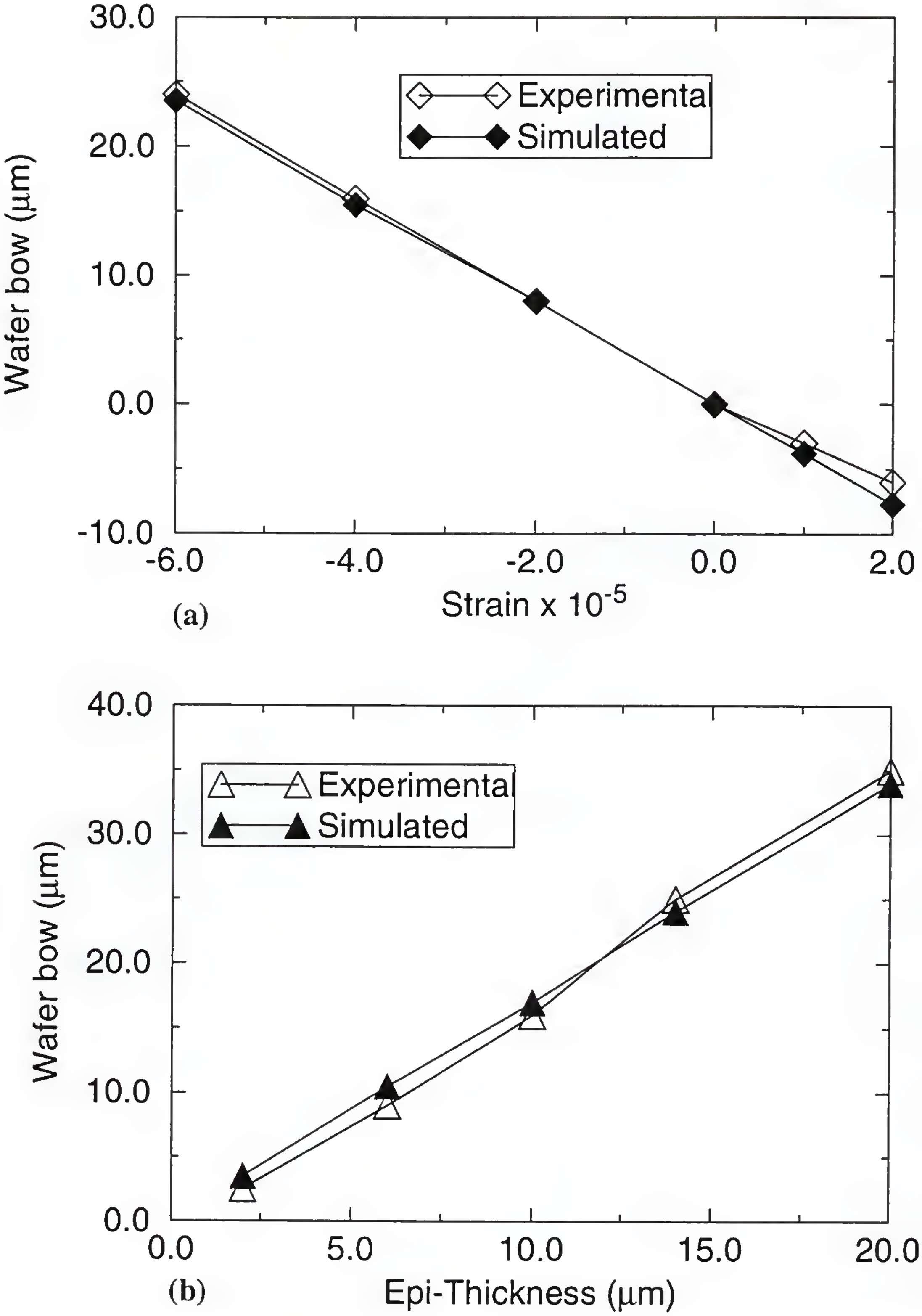


Figure 4.15 The wafer bow as a function of (a) increasing dopant concentration in the substrate for a 24 μm thick epi layer, and (b) increasing epi layer thickness.

The macroscopic simulations discussed in this section provide the user with an efficient way of determining the wafer bow for a given epi thickness and substrate doping conditions. For a given boron doping and epitaxial thickness, stress levels in the epitaxial film and the silicon substrate can also be simulated. The simulations assume that the system has not yielded to form dislocations. Thus, the stress levels given by the simulations can be used to predict when and where the loops are most likely to form. Additionally, the model can be used to simulate, and optimize a given process for the technique of "compensation."

4.3 Summary

Models based on the finite element code in FLOOPS have been developed as part of this chapter to predict stress in the silicon substrate from patterned and continuous films. Stress from patterned films was found to be a very strong function of film thickness, stripe width and intrinsic stress in the deposited film. The stress levels in the silicon substrate were also found to be sensitive to the depth in the substrate. In general, the stress levels extended deeper into the substrate for the wide stripes, but fell of rapidly if the stripes were made smaller and brought closer together. A critical ratio of the film thickness to length was found to be useful in characterizing the stress levels in the bulk. This work forms the basis of simulating the experimental data of Chapter V. The simulation results are described in Chapter VI.

A model was also developed to simulate stress from lattice mismatched epitaxial film frequently employed in silicon technology. This involved the use of a new boundary condition in the finite element code, which allowed for both the lateral and vertical deformation in the wafer. The simulated wafer bow was found to be in agreement with the experimental data. Stress levels simulated using this model could be used in predicting the onset of misfit dislocations at the epi-silicon interface.

CHAPTER V
EXPERIMENTAL INVESTIGATION OF STRESS EFFECTS FROM DEPOSITED NITRIDE STRIPES

The models developed as part of this work can be broadly classified into three main categories. In Chapter II, models for the evolution of dislocation loops in an inert ambient were developed. The simulations were compared with experimental data. Chapter III investigated stress effects from ion-implanted dislocation loops. The peak value of the simulated strain was verified from experimental data. Finally, stress from films was the focus of Chapter IV. Stress from thermal nitridation and epitaxial growth were investigated and modeled. After developing models for stress in the silicon substrate from a wide variety of sources, it is useful to investigate the effect of this stress on bulk processing properties.

Figure 5.1 illustrates a scaled MOSFET. The high dose implantation in the source and drain leads to the formation of dislocation loops in those regions. As the devices get scaled, stress effects from the nitride layers and isolation regions become important. The loop evolution during the subsequent thermal anneal could be influenced by the stress present in these areas. The loops effect device properties such as junction leakage current and may cause yield related problems. The lateral diffusion of dopants under the channel could also be affected by the presence of the stress and/or dislocation loops. Since the dopant profile in the channel directly effects device properties such as threshold voltage and sub-threshold slope, such an investigation would be useful for a technologist.

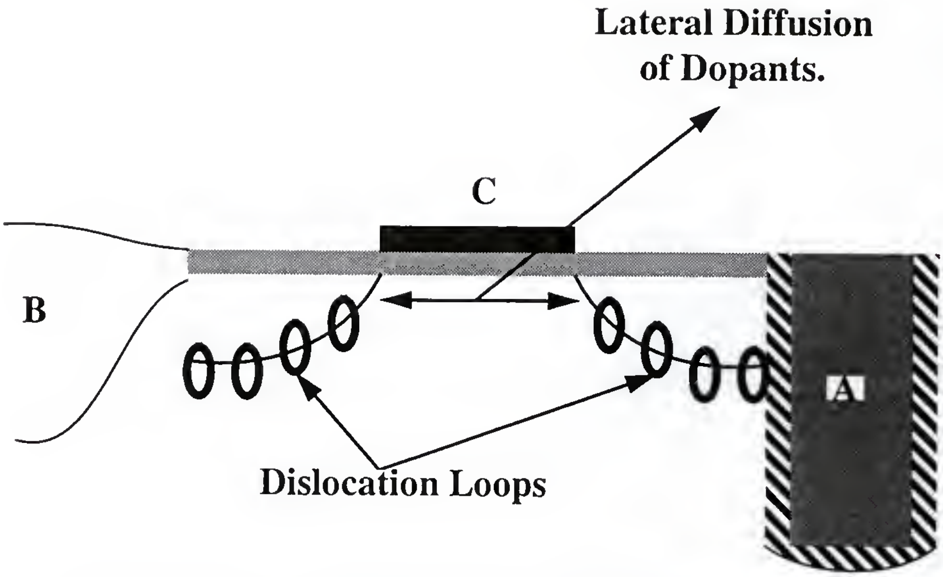


Figure 5.1 A representative diagram of a MOSFET with its possible isolation schemes, showing the location of dislocation loops and dopants. A, B, and C are the possible source of stress that may influence the evolution of dislocation loops or the diffusion of dopants.

Investigations of several researchers have revealed that phosphorus and boron exhibit retarded diffusion when annealed under a deposited nitride layer [50, 51, 54, 55]. As early as 1982, Mizuo and Higuchi [54] observed anomalous diffusion of boron and phosphorus in silicon under CVD nitride films. They discovered that in an inert atmosphere the diffusion of these dopants under CVD nitride films is retarded compared to the diffusion under the SiO_2 films covered with CVD nitride. Their results indicated that the Si-SiO_2 interface could be acting as a sink for supersaturated interstitials. However, they neglected the high levels of stress in the nitride film, and theorized that the deposited nitride film was inert, with regards to perturbing point defect concentrations in the bulk. Ahn et al. [50] observed a vacancy supersaturation and a self-interstitial undersaturation under LPCVD nitride with tensile stress. The degree of super or undersaturation of point defects was found to be closely related to the stress level in the silicon nitride film. They further theorized that the nitride film was generating vacancies by absorbing silicon atoms at the interface to relieve its own tensile stress. Osada et al. [51] investigated the effect of an LPCVD nitride on boron diffusion in the substrate below. They observed that as long as the nitride thickness was greater than 50 Å, boron diffusion was retarded under the nitride film, when compared to a region where an oxide film was under an overlying nitride. In addition, this retardation in boron diffusion was found to increase with increasing nitride film thickness and decreasing anneal temperature. The results were explained solely due to compressive stress in the substrate below the tensile deposited film, which lead to an undersaturation of vacancies. Kuo et al. [55] investigated boron diffusion in Si and $Si_{1-x}Ge_x$. They observed slower boron diffusion in compressively strained $Si_{1-x}Ge_x$, when compared to unstrained silicon, and attributed it to an increase in interstitial formation energy in the compressive $Si_{1-x}Ge_x$. However, the intrinsic boron diffusivities in $Si_{0.80}Ge_{0.20}$ and $Si_{0.90}Ge_{0.10}$ exhibited weak strain dependence, suggesting that the boron diffusivity in $Si_{1-x}Ge_x$ is predominantly a function of Ge content.

Since both phosphorus and boron diffuse mainly through an interstitial mechanism, it has been suggested that the compressive stress in the substrate immediately below the tensile nitride layer leads to an undersaturation of interstitials; which would explain the retarded diffusion. The research, described in the preceding paragraph, suggests that the stress in the nitride film has a significant effect on bulk diffusion properties. A comprehensive look at the diffusion properties of a representative dopant, as a function of film thickness and stripe width would not only greatly enhance the understanding of stress-assisted diffusion, but also allow calibration of process simulators like FLOOPS. In order to facilitate such a study, it is important to introduce stress in the silicon substrate in a predetermined way. Simulations in Chapter IV revealed that patterned nitride films introduce both compressive and tensile stress in the substrate. The stress levels in the substrate are a strong function of nitride film thickness and stripe width. Thus, such structures would be extremely useful in observing the effect of both compression and tension simultaneously on bulk processing variables. In contrast to the work of Ahn et al. [50], results from such a study could be analyzed directly using the finite element stress solver in process simulators like FLOOPS.

The discussion in the preceding paragraphs focussed on stress-assisted diffusion of phosphorus and boron; the kinetics being dominated by point defect concentrations in the bulk. With extensive use of ion-implantation in modern devices, type-II loops are frequently encountered in silicon technology. Since dislocation loop evolution is strongly governed by point defects concentrations in the bulk, it seems reasonable to assume that stress in the substrate would have some effect on the evolution kinetics of ion-implanted dislocation loops. For example, a trench is known to introduce both compressive and tensile stress in substrate adjacent to it (Figure 5.1). An experiment which simultaneously investigates the effect of compression and tension on the evolution of dislocation loops, would, therefore, be of great aid to process and device engineers designing new devices or improving old ones. To illustrate this point further, assume that compressive stress, which causes an undersaturation of self interstitials, also causes the loops to dissolve faster in time. Engineers could then use this property to design trenches which introduce compressive stress in regions of the active device where it is useful to reduce the density of dislocation loops. The remaining portion of this chapter discusses the design and results of an experiment which investigates some of the stress related issues discussed in this section.

An experimental procedure is designed to investigate the effects of stress on the evolution of dislocation loops and on the diffusion of phosphorus as a representative dopant. Undersaturation of interstitials in a compressive pressure field was discussed in Chapter IV. A series of nitride stripes of the type discussed in Chapter IV are used to generate alternating tensile and compressive stress fields in the substrate. The diffusion of phosphorus under the masked and unmasked regions is compared using the standard junction staining technique. The evolution of the dislocation loops with anneal time is monitored using Transmission Electron Microscopy (TEM) technique used in Chapters II and III. Although both the phosphorus diffusion and dislocation loop experiments were performed in parallel, for the sake of clarity they are discussed in separate sections.

5.1 Effect of Patterned Nitride Stripes on the Diffusion of Phosphorus in Silicon

5.1.1 Experimental Details

P-type boron doped (15-25 Ω resistivity) Czochralski, <100> oriented wafers were used for the study. The wafers were annealed in dry oxygen for 60 minutes to grow a 300 Å oxide. Ellipsometric measurements were used to confirm that the thickness of the oxide did not change appreciably on the same wafer, and from wafer to wafer. The oxide was initially used as a screen for subsequent ion-implantation and later used as a diffusion mask to prevent the loss of dopant during annealing. A Varian ion-beam implanter was used to implant phosphorus into the silicon substrate through the screen oxide. A low dose ($1\times10^{14}/cm^2$) was used to eliminate high diffusion effects during the anneal. The energy of the implant (100 keV) was chosen to match standard implantation procedures in modern CMOS processes. Under these implant conditions the dopant redistributed itself in a 1 μm deep region in the silicon substrate. This would aid subsequent cleaving of the samples for junction depth measurements. The wafers were then subjected to a 30 minute/900°C anneal to remove the implantation damage and activate the implanted dopant.

A spin on technique (3500 rpm/25 second) was used to deposit an I-line photoresist on the oxide coated wafers. A photolithographic stepper then patterned stripes ranging in width from 1-1000 μm on the photoresist. Using the photoresist as a mask, a 10:1 buffered hydrofloride etch was employed to create the corresponding stripes in the oxide layer. The lateral etch was insignificant since the thickness of the oxide was 0.03 μm. The remaining photoresist was then removed by boiling the wafers in 110°C solution of sulfuric acid and hydrogen peroxide.

A LPCVD (Low Pressure Chemical Vapor Deposition) silicon nitride was deposited on the wafers to generate the stress in the substrate. The nitradation was performed at 900°C/211 mTorr. The following flow rates were used for the various gases during the process; Nitrogen: 48 sccm; $SiHCl_2$: 60 sccm; Ammonia: 882 sccm. The flow rates were chosen to match stress calibrated nitrides found in literature [17, 50]. Under these conditions it is estimated that the stress levels in the nitride are of the order of $4x10^{10}$ dynes/cm^2. Simulations in FLOOPS (Chapter IV) suggest that this would generate sufficient stress in the silicon substrate to observe the effects under investigation. However, the stress levels would remain below the yield strength of silicon. Therefore, the possibility of the diffusion being effected by dislocations is minimized. The samples were subsequently annealed in a nitrogen ambient at 1000°C for times ranging from 2 to 4 hours. A flow chart depicting the experiment is shown in Figure 5.2.

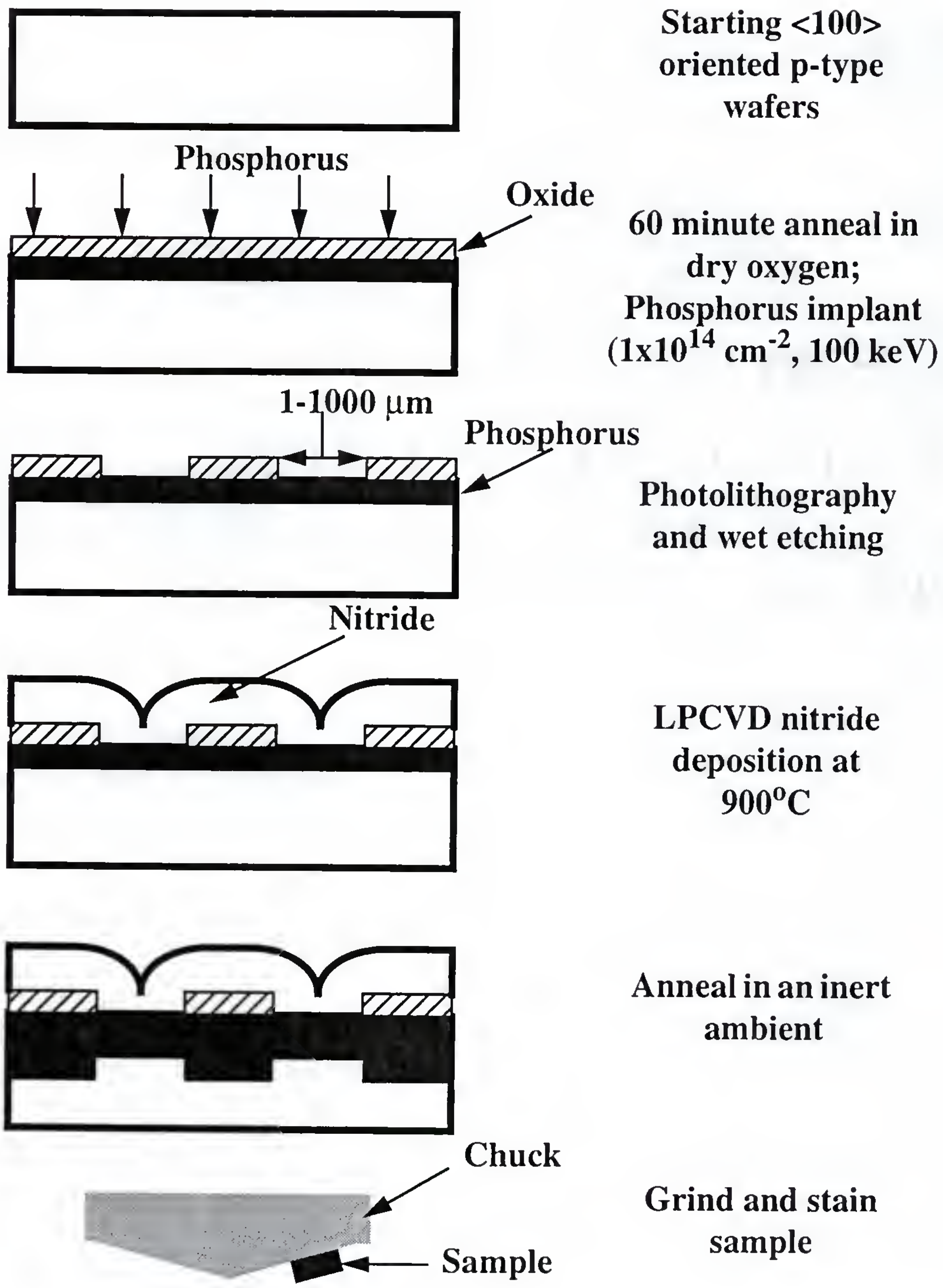

Starting <100> oriented p-type wafers
Phosphorus
Oxide
60 minute anneal in dry oxygen; Phosphorus implant ($1x10^{14}$ cm^{-2}, 100 keV)
1-1000 μm
Phosphorus
Photolithography and wet etching
Nitride
LPCVD nitride deposition at 900°C
Anneal in an inert ambient
Chuck
Sample
Grind and stain sample

Figure 5.2 Flow schematic of the experiment designed to study the effect of nitride stripes on the diffusion of phosphorus in silicon.

5.1.2 Junction Staining

As discussed in the beginning of this chapter, compressive stress below the nitride stripes and tensile stress outside the stripes would alter the diffusion kinetics of the dopant. Since the dimensions of the stripes range from 1 to 1000 μm, a convenient method to quantify the diffusion is the junction staining technique which chemically demarcates the p-n junction. In essence, this staining technique involves cleaving the samples in depth and then chemically staining the n-type dopant.

The samples were initially cut into ~3 mm square pieces. They were mounted on a stainless steel chuck with a cleaving angle of ~17 minutes. The angle was chosen in view of the fact that the predominant diffusion is within a micron of the surface. A diamond compound on a glass plate was used as the grinding surface. Upon cleaving, a chemical solution was used to demarcate the n-type dopant (Figure 5.3). The samples were placed under an optical microscope and diffraction patterns used to extract the exact angle of the cleave. The micrometer scales on the microscope were employed to calculate the lateral variation in junction depth for all samples (Figure 5.4).

Though the use of concentration profiling techniques such as SIMS are more accurate in extracting diffusion properties of dopants in silicon, they present technical difficulties when profiles at lateral dimensions less than a micron are required. Ideally, a two dimensional concentration profiling technique such as scanning capacitance microscopy would be best suited in extracting the quantities of interest from the annealed samples. Since the objective is not to compare diffusion in two different samples, but to observe variations in phosphorus diffusion kinetics from regions of compression to regions of tension in the same sample, junction staining offers a good means to quantify this effect.

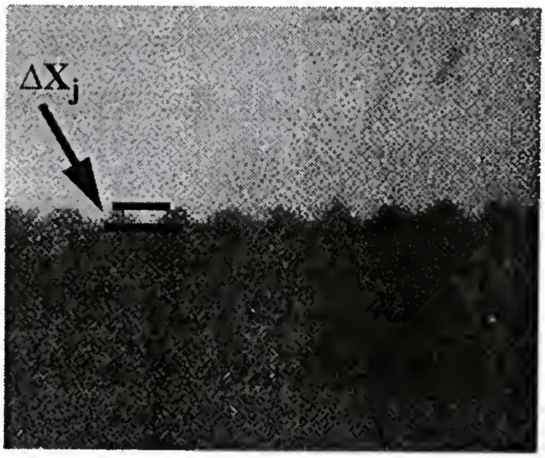


Figure 5.3 Picture illustrating the stained phosphorus junction in the silicon substrates. Note the retarded diffusion under the nitride stripes (~20 μm wide).

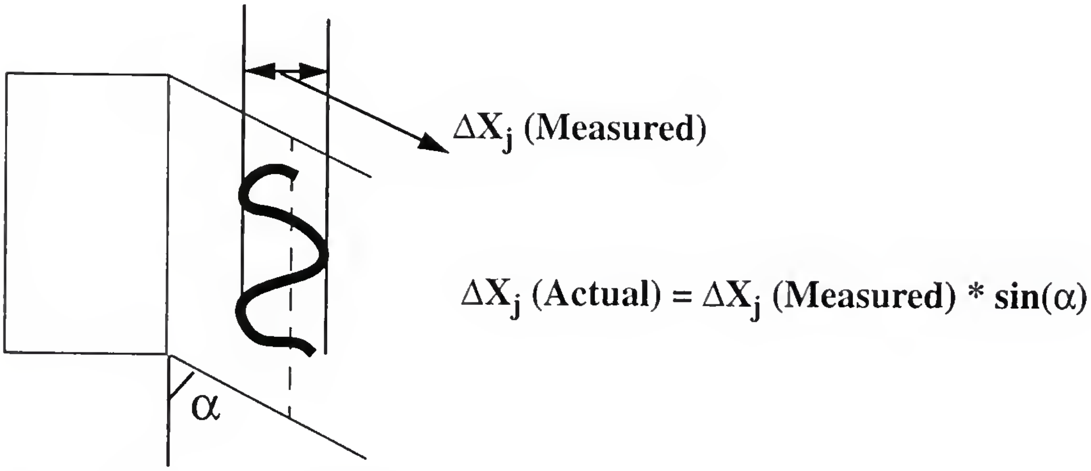

ΔX_j (Measured)
ΔX_j (Actual) = ΔX_j (Measured) * sin(α)
α

Figure 5.4 Schematic illustrating the extraction technique for ΔX_j.

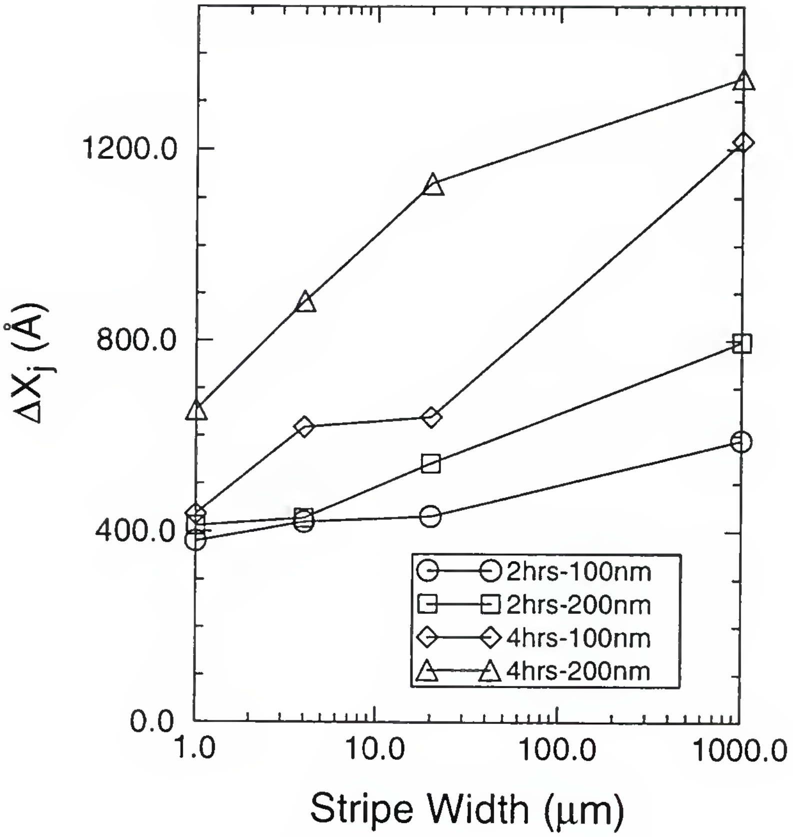


Figure 5.5 A plot of the net retardation of phosphorus diffusion under the nitride stripes as a function nitride stripe width thickness for different anneal conditions.

5.1.3 Experimental Results and Analysis

Figure 5.5 illustrates the effect of the nitride stripes on the diffusion of phosphorus in silicon, which is quantitatively represented as ΔX_j. It is the difference between the junction depth under a nitride stripe (i.e. the region where the nitride is directly on top of the silicon) and outside it (i.e. the region where an oxide layer is padded between the nitride layer and the silicon substrate). The trends are quite apparent. As the thickness of the nitride layer is increased, the net retardation (ΔX_j) also increases. An increase in the stripe width for the same nitride thickness also causes ΔX_j to increase. These results call for further discussion.

Simulations in Chapter IV suggested that increase in the thickness of the deposited nitride layer would lead to higher levels of stress in the substrate below the layers. This explains the added retardation observed in the experimental data as the thickness of the nitride layer was increased. The results, however, do not agree with data of Ahn et al. [50]. In their study the retardation was found to remain constant with increase in thickness of the nitride layer. However, they did observe a marked decrease in the net retardation as the width of the stripe was reduced, which concurs with the results of this study.

An increase in width of the nitride stripes, with the thickness remaining the same, leads to a decrease in the stress levels in the substrate in regions close to the interface. This was corroborated by the simulations in Section 4.1.4. Therefore, with a tensile intrinsic stress in the nitride film, it is expected that the compressive pressure immediately below the nitride stripe would increase as the stripes are brought closer together (i.e. made smaller). This would decrease the local equilibrium concentration of interstitials in the region immediately below the nitride layer. Since phosphorus is known to diffuse mainly through an interstitial phenomenon, it is expected that the net retardation (ΔX_j) would increase as the stripes are made smaller and brought closer together. The results of this study, however, suggest some competing phenomenon is at work. A first order analysis of this phenomenon is presented in the subsequent paragraph.

The stripe width dependent stress analysis presented in the preceding paragraph is true for regions that are very close to the silicon/silicon-nitride or silicon/silicon oxide interface. For regions deeper in the substrate, the stress levels increase with increasing stripe width (Section 4.1.4). Since the junction staining technique is sensitive only to the junction depth in the sample, this competing mechanism is responsible for the increase in the net retardations with increasing stripe width. For the one micron stripe width samples the net retardation (ΔX_j) falls to ~ 400 Å, and is at the resolution limit of the junction staining technique. For the widest stripes (1000 μm), the retardation increases almost three fold, to ~ 1300 Å.

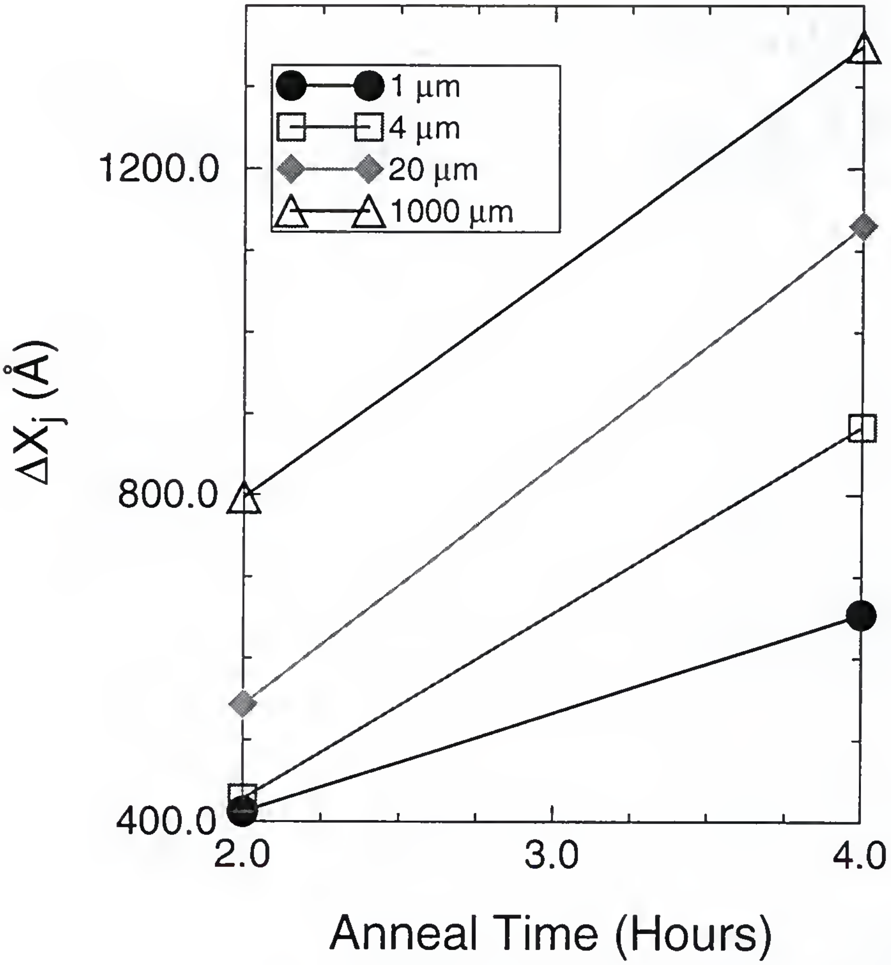


Figure 5.6 Plot illustrating the increase in the net retardation (ΔX_j) with time, of phosphorus diffusion under a nitride layer for varying stripe widths.

Figure 5.6 illustrates the effect of increasing anneal times (at 1000°C) on the net retardation of phosphorus diffusion (ΔX_j). For all stripe widths the retardation shows a marked increase with time, indicating that the nitride continues to retard the diffusion of the dopant for large diffusion times. Thus, these results give a first order look at the relaxation kinetics of the deposited nitride film. For the LPCVD deposited nitride, as indicated by a distinct increase in ΔX_j, it is apparent that there is little or no relaxation in strain with time.

Since the anneal was done at 1000°C, and the nitride deposited at 900°C, a substantial thermal mismatch strain exists between the deposited nitride and the compressed substrate below. It is useful to investigate the magnitudes of the various components of the stress in the silicon substrate. The total film stress is

$$\sigma_f = (\alpha_s - \alpha_f)\left(\frac{Y_f}{1 - \nu_f}\right)(T - T_{dep}) + \sigma_{dep} \qquad 5\text{-}1$$

where σ_f is the stress in the nitride film, α_s and α_f are thermal expansion coefficients of the silicon substrate and the nitride stripe respectively, Y_f and ν_f are the Young's modulus and Poisson's ratio respectively of the nitride stripe, T is the anneal temperature (=1000°C), T_{dep} is the temperature at which the nitride layer was deposited (= 900°C), and σ_{dep} is the stress of the nitride film when it was deposited, i.e. the intrinsic stress. The analysis indicates that the thermal component is a significant fraction of the total stress in the nitride film. A simulation procedure for the stress-assisted phosphorus diffusion, incorporating the aforementioned effects, is described in Chapter VI.

5.2 Effect of Patterned Nitride Stripes on the Evolution of Dislocation Loops in Silicon

Section 5.1 discussed the effect of patterned nitride stripes on the diffusion kinetics of phosphorus. In this section, experimental results from a parallel experiment are presented. The major difference between the two experiments is that instead of implanting low dose phosphorus, high dose silicon is implanted into the silicon substrate to form dislocation loops. The loops are then annealed in an inert ambient to observe the effect of the patterned nitride films on their evolution.

5.2.1 Experimental Details

P-type boron doped (15-25 Ω resistivity) Czochralski, <100> oriented silicon wafers were used for the study. The wafers were annealed in dry oxygen for 60 minutes to grow a 300 Å oxide. Ellipsometric measurements were used to confirm that the thickness of the oxide did not change appreciably on the same wafer, and from wafer to wafer. The oxide was initially used as a screen for subsequent ion-implantation and later used as a diffusion mask to prevent loss of damage during annealing. A Varian ion-beam implanter was used to implant silicon into the silicon substrate through the screen oxide. A high dose ($2\text{x}10^{15}/\text{cm}^2$) was used to amorphize the substrate. The energy of the implant (100 keV) was chosen to match standard implantation procedures to form type-II dislocation loops. Under these implantation conditions the silicon substrate is amorphized to a depth of ~1500Å. End-of-range (type-II) loops are formed during the subsequent anneal at this depth.

Using a photolithography and wet etching technique described in section 5.2.1, the oxide was etched to form stripes ranging in width from 1 to 1000 μm. A LPCVD (Low Pressure Chemical Vapor Deposition) silicon nitride was deposited on the wafers to generate the stress in the substrate. The nitridation was performed at 900°C/211 mTorr. Detailed deposition conditions are given in section 5.2.1. Under these conditions it is estimated that the stress levels in the nitride are of the order of 4×10^{10} dynes/cm^2. Simulations in FLOOPS (Chapter IV) suggest that this would generate sufficient stress in the silicon substrate to observe the effects under investigation. However, the stress levels would remain below the yield strength of silicon. The samples were then annealed in a nitrogen ambient at 900°C for one and a half hours. A flow chart depicting the entire experiment is shown in Figure 5.7.

5.2.2 Transmission Electron Microscopy

The silicon implanted samples were mechanically lapped and jet etched for observation under a JEOL 200CX TEM. The analysis was performed using weak-beam dark field (g_{220}) image of the samples. By measuring loop size and their numbers in plan view, it was possible to determine quantitatively the total density of the loops, their radii, and the concentration of atoms trapped in the loops. Assuming a circular loop, the radius of each loop was measured along its longest axis and the corresponding loop area was calculated. The concentration of atoms bound by the loops is estimated by multiplying the fraction of the loop area by the atomic density in the <111> plane (1.5×10^{15} / cm^2).

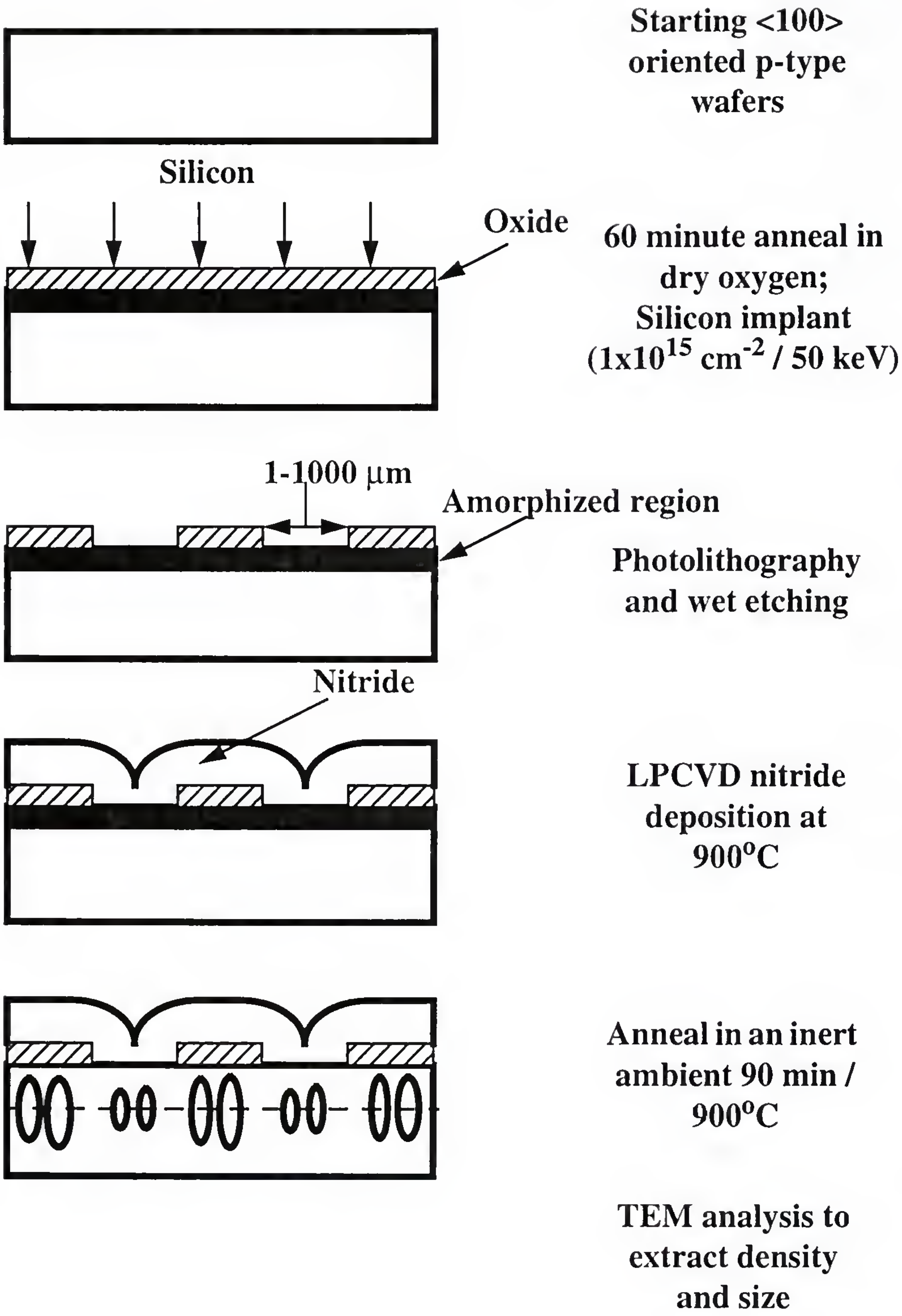

Starting <100> oriented p-type wafers
Silicon
Oxide
60 minute anneal in dry oxygen; Silicon implant (1x10^15 cm^-2 / 50 keV)
1-1000 µm
Amorphized region
Photolithography and wet etching
Nitride
LPCVD nitride deposition at 900°C
Anneal in an inert ambient 90 min / 900°C
TEM analysis to extract density and size

Figure 5.7 Flow schematic of the experiment designed to study the effect of nitride stripes on the evolution of ion-implanted dislocation loops in silicon.

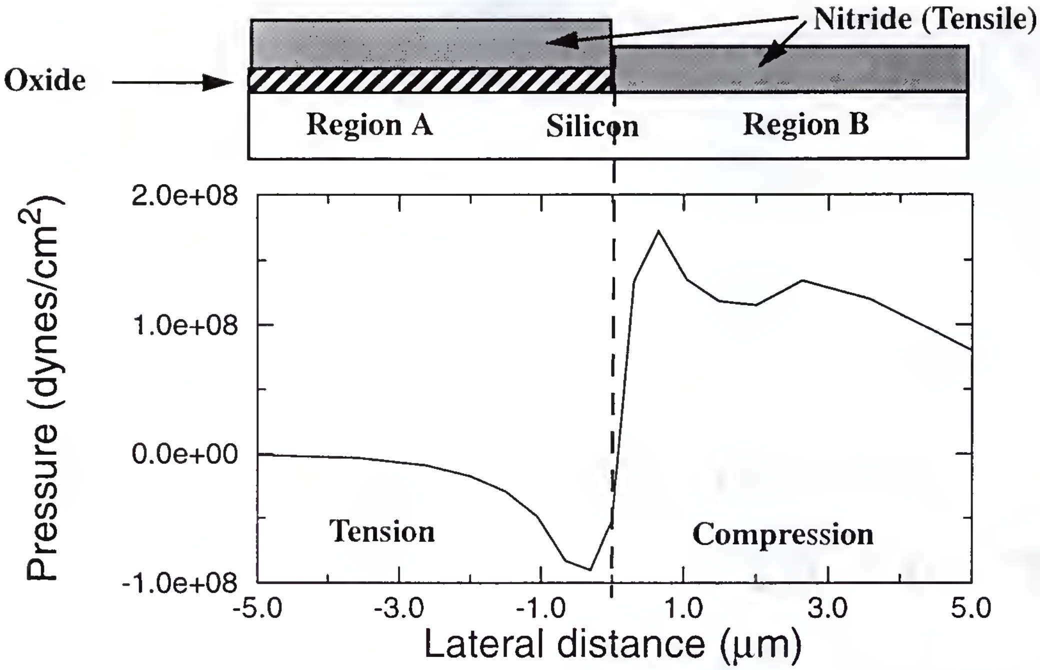
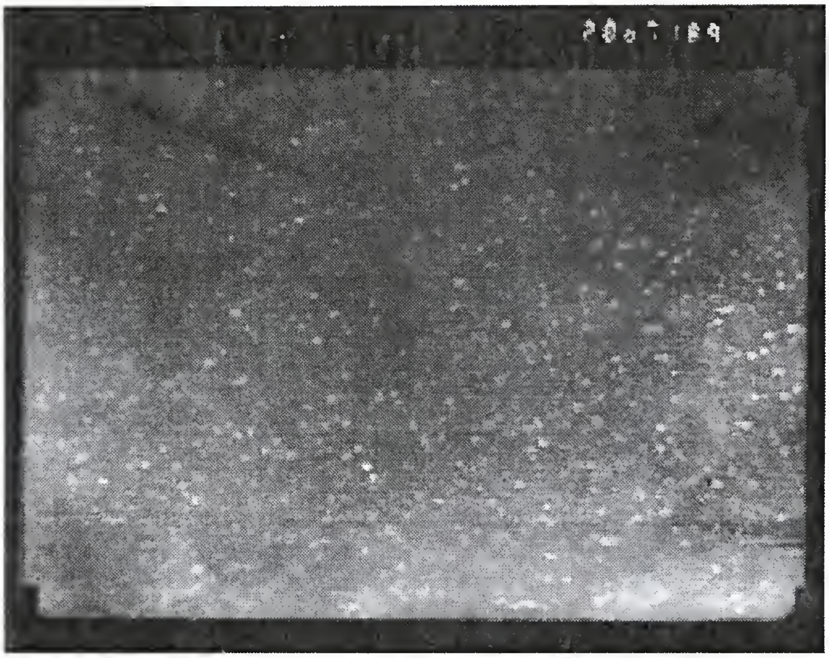


Figure 5.8 Finite element simulation of the hydrostatic pressure under a nitride stripe in FLOOPS illustrating the regions of compression (under nitride) and tension (under the oxide padded nitride).

A major challenge while investigating loop ensemble properties was to extract their lateral variation in the same sample. For the 1000 μm wide stripes, two different samples were prepared for TEM analysis; one under the nitride layer (Region A - Figure 5.8) and the other under the oxide-nitride layer (Region B - Figure 5.8). For the 20 μm stripe widths a representative sample from each lot was chosen and prepared for TEM. The sample was visually (i.e. under TEM) investigated for variations in dislocation loop size and density. Once these areas were identified, microphotographs were taken from two regions in the sample, by moving exactly 20 μm in real space. The procedure was simpler for the 4 μm samples. A matrix of microphotographs encompassing an area of 10 x 10 μm^2 was taken. A single photograph was sufficient to extract the loop ensemble properties under the 1 μm nitride stripes.



10.1	8.6	8.3	10.1	10.8	**9.6**
8.1	7.4	7.6	8.5	10.6	**8.4**
10.4	10.1	9.8	10.1	10.1	**10.1**
8.0	8.4	7.6	8.2	8.2	**8.2**

Figure 5.9 Dark field plan view TEM microphotographs (x 20,000 magnification) for a sample with nitride stripe width of 1 μm, and a thickness of 1000 Å. The stripes are running from left to right. The matrix below indicates the density ($x10^9/cm^2$) for each square micron in the microphotograph. The numbers on the right are the average for each row.

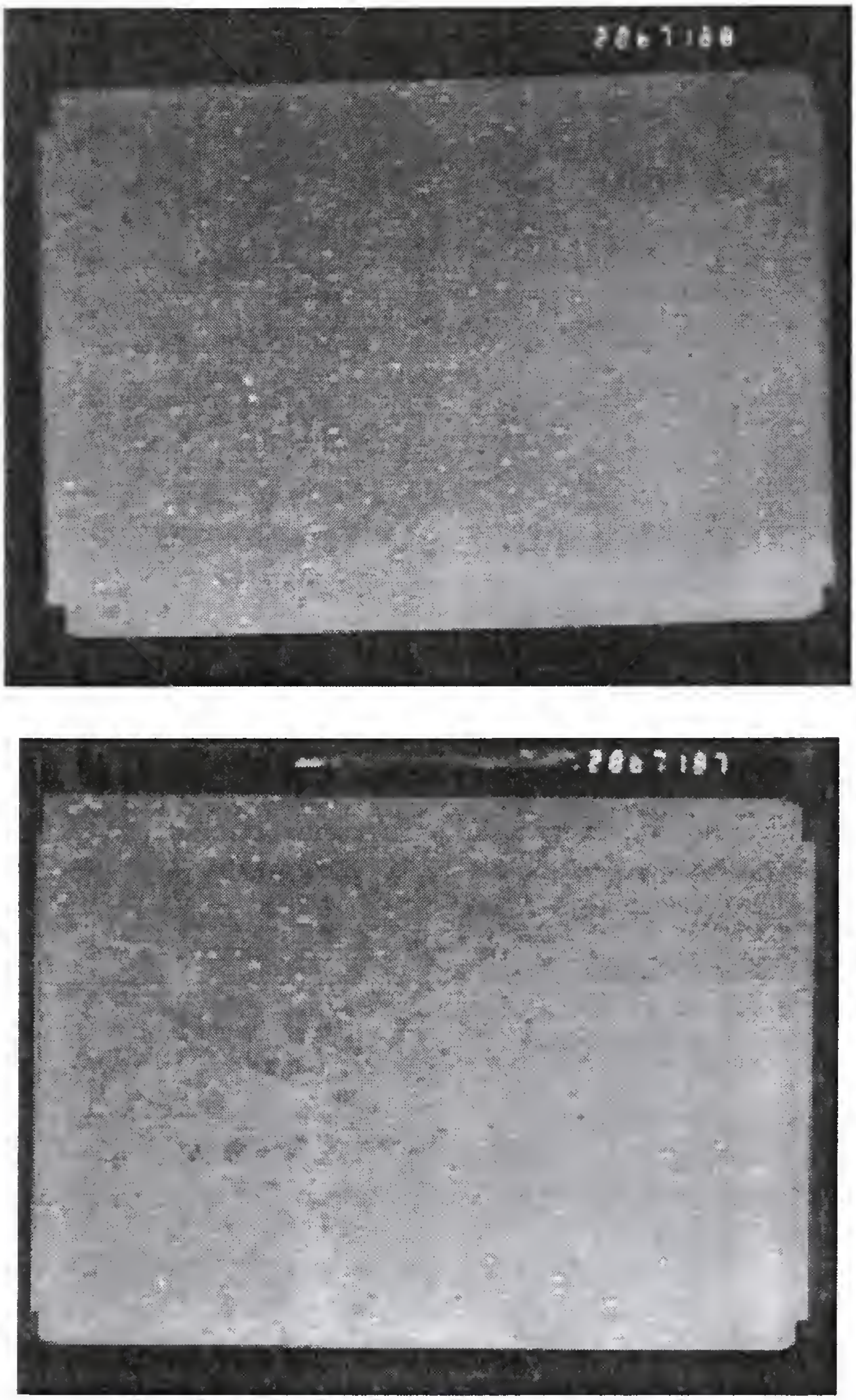


Figure 5.10 Dark field plan view TEM microphotographs (x 20,000 magnification) for a sample with nitride stripe width of 4 μm, and a thickness of 1000 Å. The stripes are running from top to bottom in both photographs. Note the fall in loop density and size from left to right.

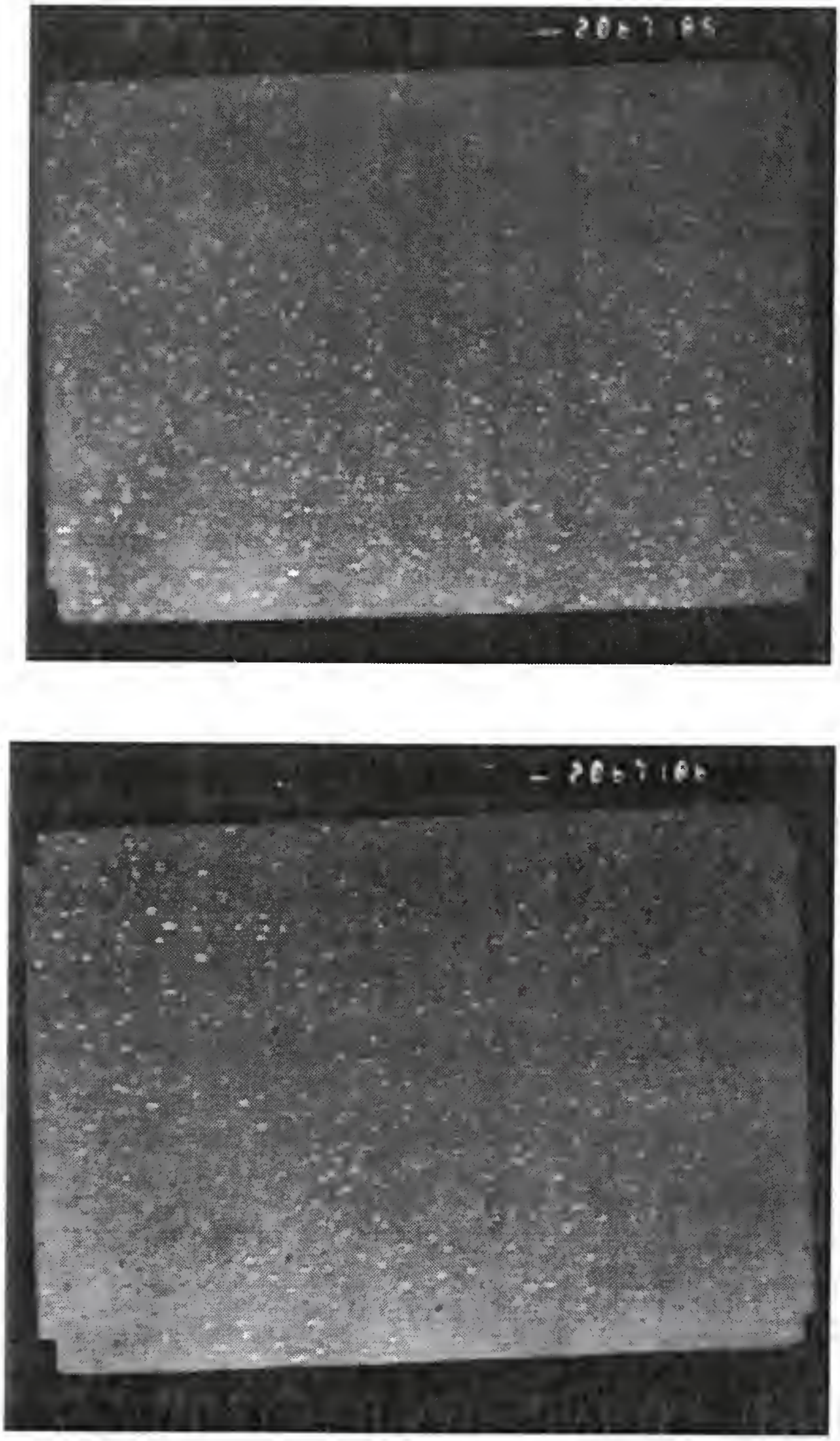


Figure 5.11 Dark field plan view TEM microphotographs (x 20,000 magnification) for a sample with a nitride stripe width of 4 µm, and a thickness of 1000 Å. The stripes are running from top to bottom in both photographs. Note the fall in loop density and size from left to right. The photographs are from a different region from the one showed in Figure 5.10.

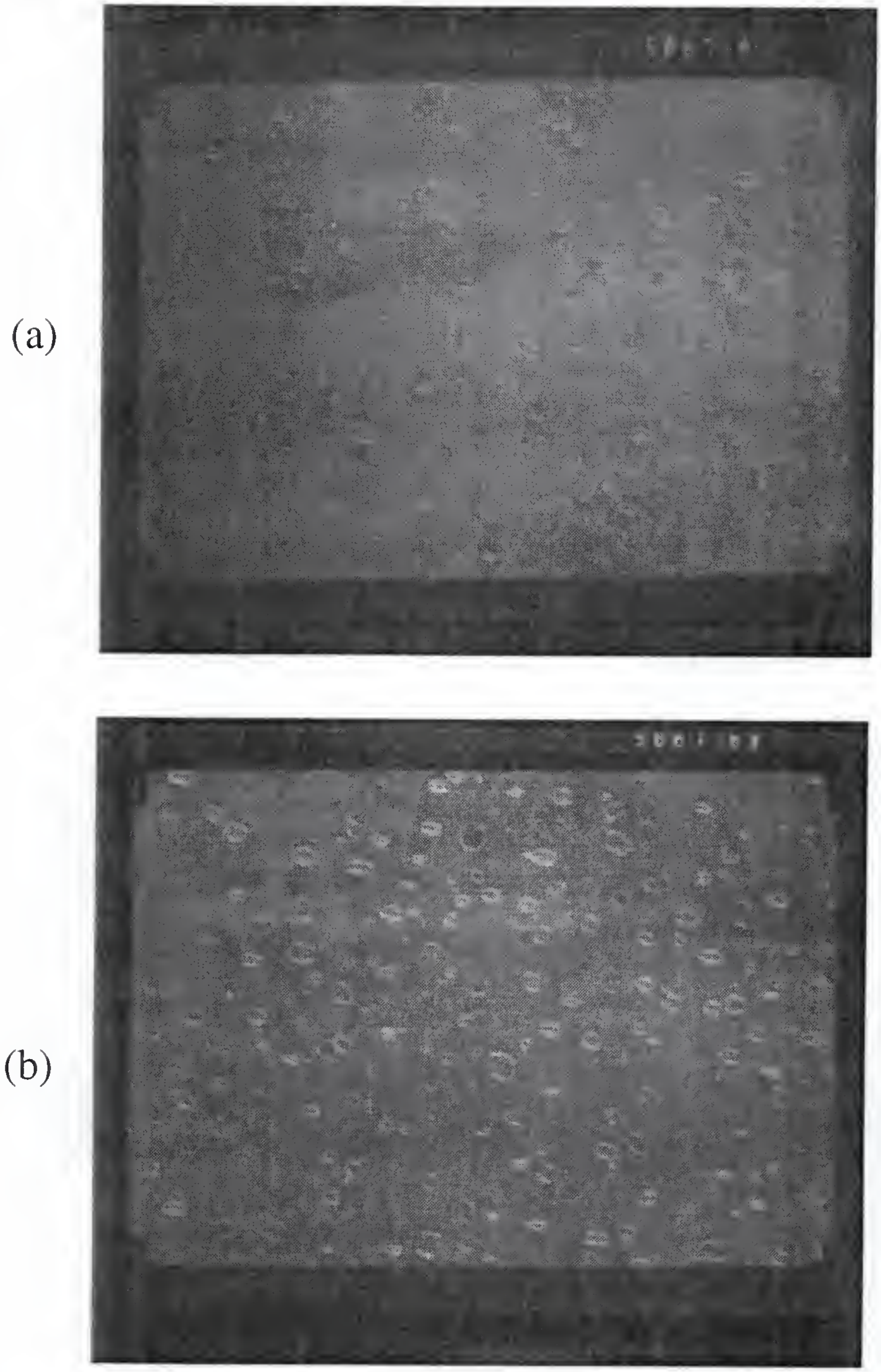


Figure 5.12 Dark field plan view TEM microphotographs (x 50,000 magnification) for a sample with a nitride stripe width of 20 μm, and a thickness of 1000 Å; under (a) compressive (region - A), and (b) tensile (region - B) regions. Note the significant difference in the size and density of the loops in the two regions.

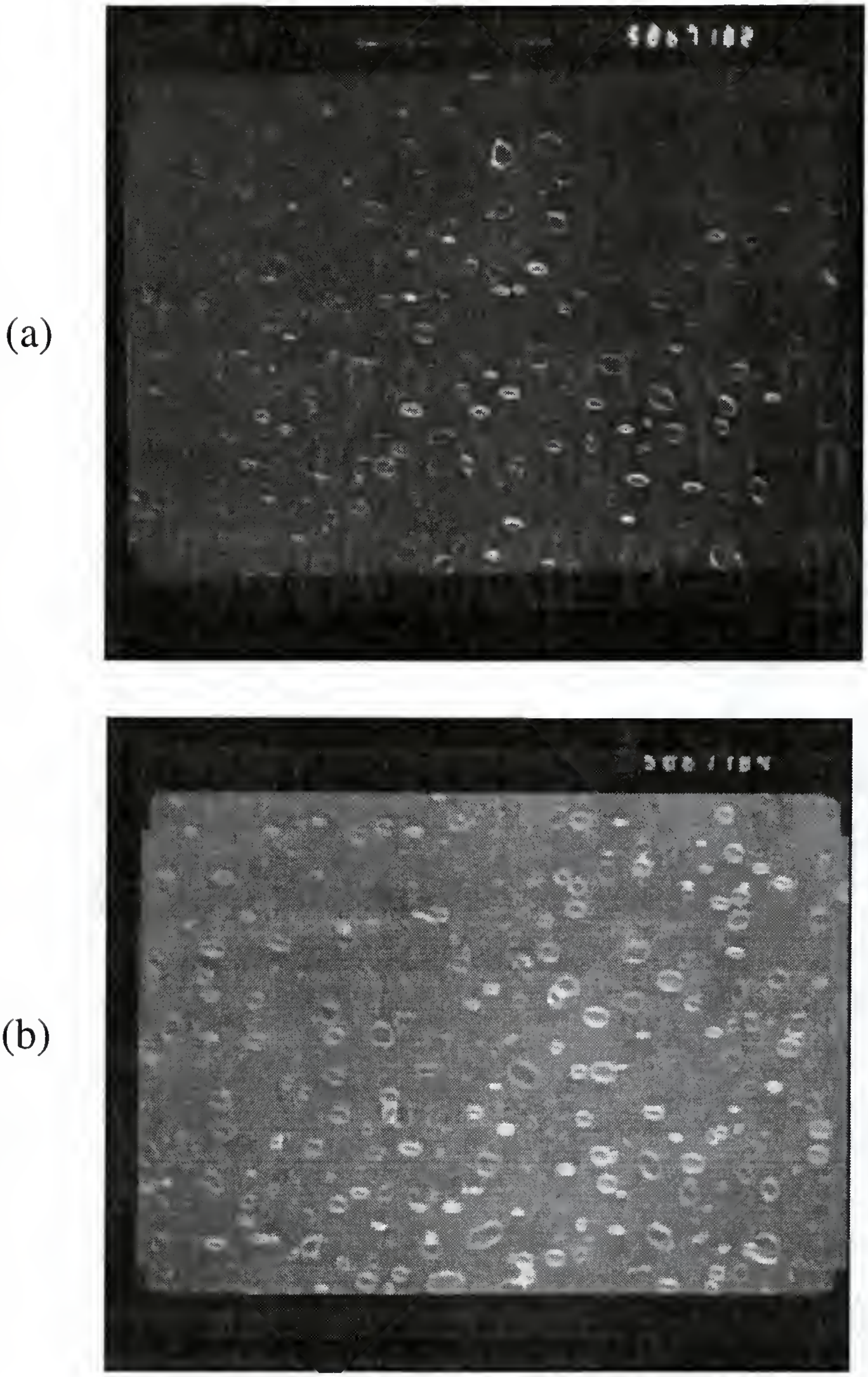


Figure 5.13 Dark field plan view TEM microphotographs (x 50,000 magnification) for a sample with a nitride stripe width of 20 μm, and a thickness of 1000 Å; under (a) compressive (region - A), and (b) tensile (region - B) regions. The photographs are from the same sample shown in Figure 5.12, but from a different region.

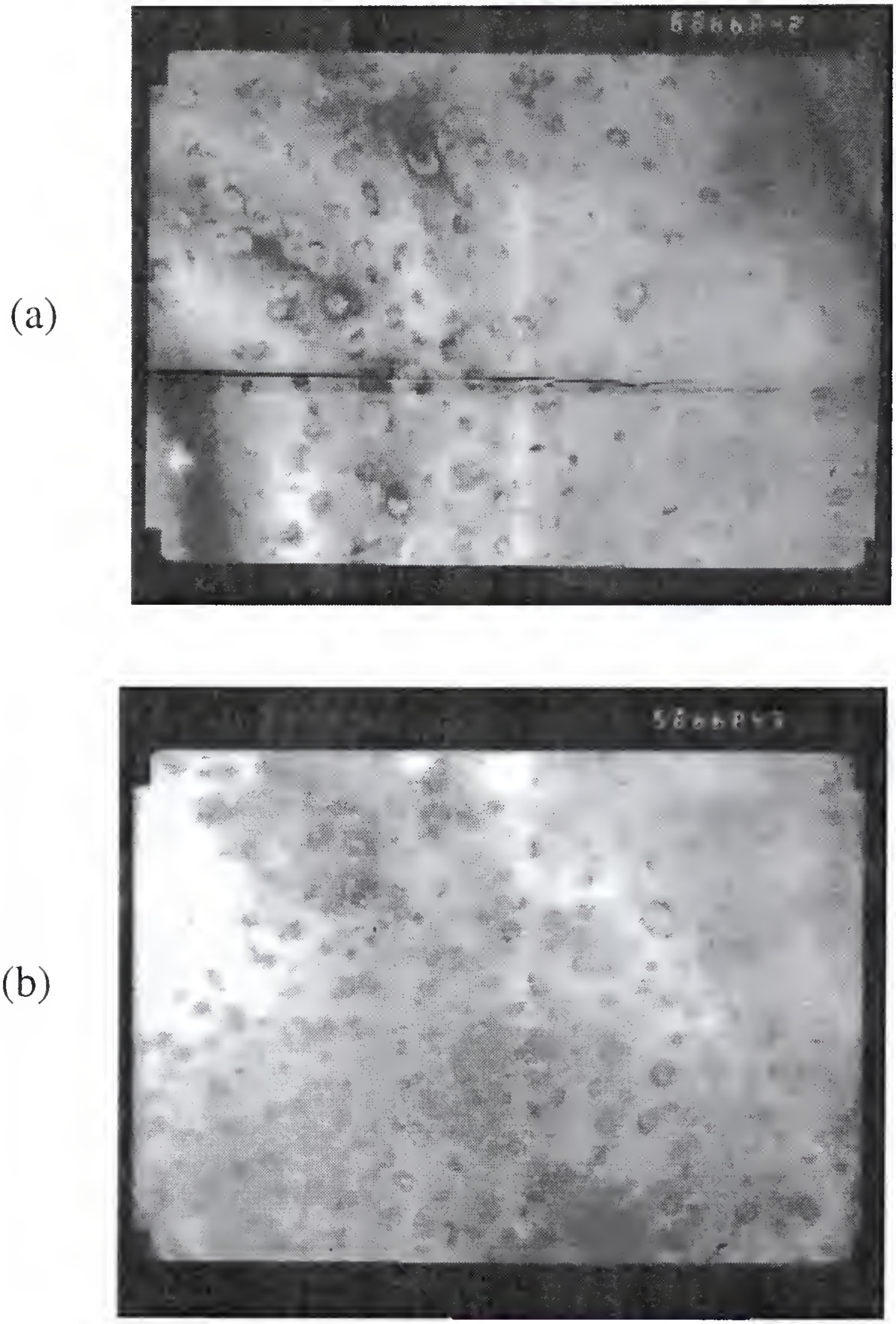


Figure 5.14 Dark field plan view TEM microphotographs (x 50,000 magnification) for a sample with a nitride stripe width of 1000 µm. and a thickness of 1000 Å; under (a) compressive (region - A), and (b) tensile (region - B) regions. Note that the difference in the loop density or radius is not very apparent visually.

5.2.3 Experimental Results and Analysis

Two fundamental figures of merit used to quantify a dislocation loop ensemble are its total density (D_{all}) and the average radius (R_{ave}). Earlier work quantified their evolution in an inert ambient [Chapter II]. This study focuses on the net variation in these quantities from region A to region B (Figure 5.8). Figure 5.9 to Figure 5.14 show dark field plan view TEM microphotographs of the samples with stripe widths varying from 1 to a 1000 microns. The thickness of the nitride film is 1000 Å, and the samples were annealed for 90 minutes at 900°C. The loops are consistently found to be sparser and smaller under a nitride layer, i.e.

$$D_{all}(A) > D_{all}(B) \qquad 5\text{-}2$$

$$R_{ave}(A) > R_{ave}(B) \qquad 5\text{-}3$$

These results are consistent with the hypothesis in Section 5.1.3 that a compressive stress field in region B forces an increase in the equilibrium concentration of vacancies. Under these conditions an interstitial inside the loop is more likely to leave the ensemble and recombine with a vacancy outside the loop, or a vacancy might move into the loop and cause it to shrink. A reverse phenomenon is in effect in region A, which leads to bigger and denser loops in that region.

The general procedure for characterizing dislocation loop ensembles in silicon was discussed in detail in Chapter II. The peak radius (R_{peak}), average radius (R_{ave}), the density of loops with peak radius (D_{peak}), and the total density of loops (D_{all}), were used to characterize a dislocation loop ensemble. This procedure works well if the objective is to quantify the time evolution of a dislocation loop ensemble. However, in this experiment the goal is to investigate the stress-assisted evolution of dislocation loops. In particular, the focus is on the change in the properties of the loop ensemble from regions of compression (Region B) to regions of tension (Region A). To explain the effects observed in the experimental data the following three quantities are defined:

(i) $\mathbf{\Delta D_{all}}$ ⇒ Total density of loops in region A - Total density of loops in region B.

(ii) $\mathbf{\Delta R_{ave}}$ ⇒ Average radius of loops in region A - Average radius of loops in region B.

(iii) $\mathbf{\Delta N_{trap}}$ ⇒ Total number of trapped atoms in region A - Total number of trapped atoms in region B.

Figure 5.15 illustrates this net variation in ΔD_{all} and ΔR_{ave} as a function of the stripe width. As the stripes are brought closer together the net variation in the total density of the dislocation loops increases (for most cases), while the net variation in the average loop radius diminishes. Though the variation in ΔD_{all} is within error bars, the trend for the change in ΔR_{ave} is quite evident. The fall in ΔR_{ave} with increasing stripe width may be due to the fact that interstitials released from dissolving loops in the compressed regions need to travel a larger distance before they can contribute to the growth of the loops in the tensed regions. This phenomenon is more dominant at the smaller stripe widths, as the diffusion lengths of point defects are larger than the stripe widths, under the anneal conditions used.

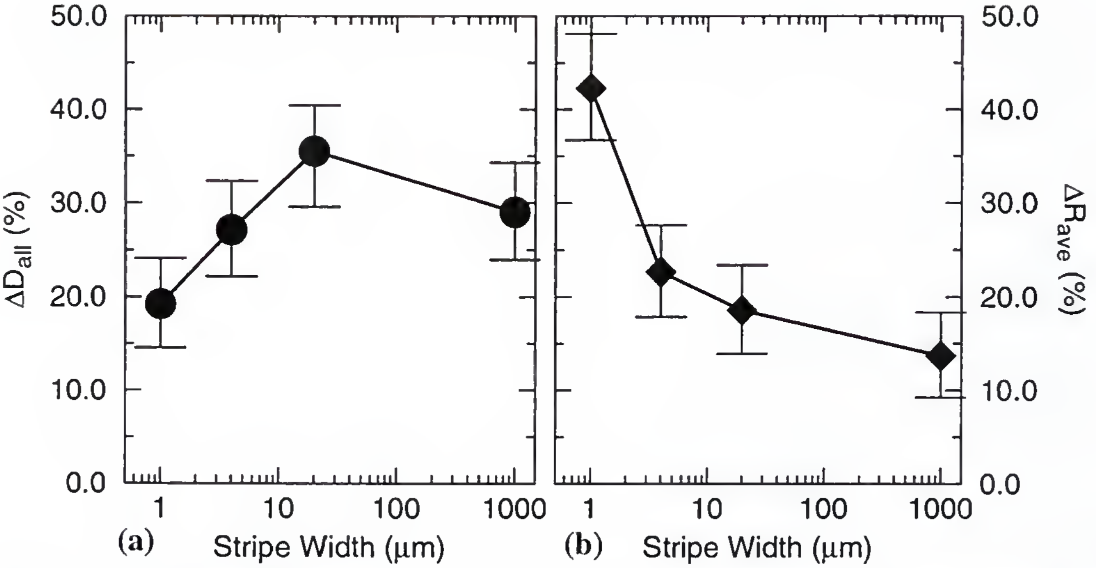


Figure 5.15 The net variation (as a function of the stripe width) in (a) total density, and (b) average radius of the dislocation loop ensemble, from a region where the nitride is directly on top of the silicon substrate to a region where an oxide layer pads of the underlying silicon from the deposited nitride.

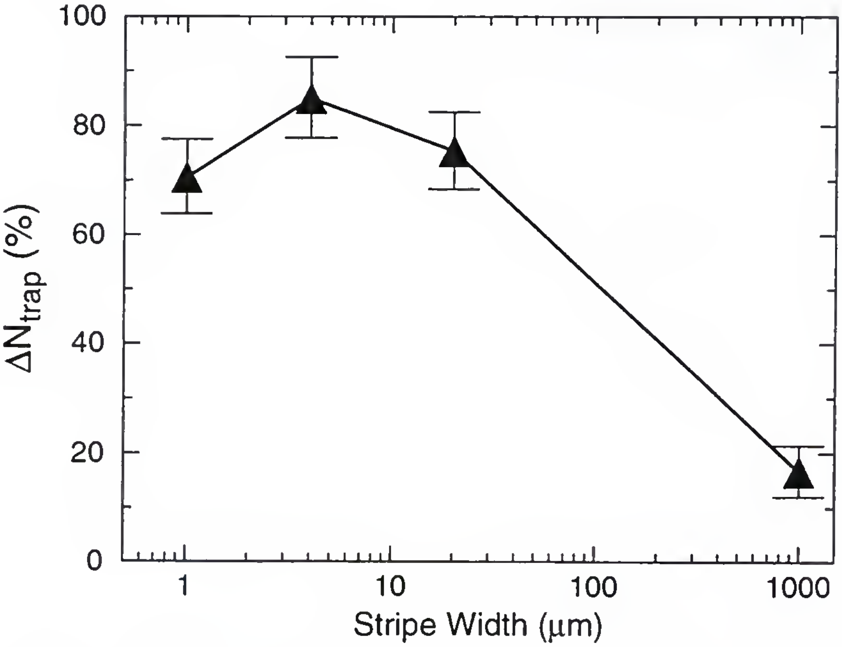


Figure 5.16 The net variation (as a function of the stripe width) in the total number of trapped atoms in the dislocation loop ensemble, from a region where the nitride is directly on top of the silicon substrate to a region where an oxide layer pads of the underlying silicon from the deposited nitride.

Though the total density and average loop radius are of great interest to the technologist, better insight into the physics is obtained by studying Figure 5.16. The net variation in the number of trapped interstitial in the ensemble is substantial (~75%) for the thinner stripes. For the case of widest stripe (~1000 µm) the variation is down to ~ 20%. It appears that under the anneal conditions used in this experiment, the interstitials from the compressed regions (Region B) are able to diffuse laterally across to the tensed regions (Region A) for the smaller stripe widths, while for the case of the widest stripes, such a communication is not possible. This hypothesis explains the small difference in the number of trapped interstitials from region A to region B for the case of the 1000 µm stripe width samples.

A simulation procedure, based on the models developed in Chapters II and IV, is described in Chapter VI. Some of the physics discussed in this section is quantified as part of this simulation work.

5.3 Summary

A experimental procedure was designed to investigate the stress-assisted diffusion of phosphorus and the evolution of ion-implanted dislocation loops. In the compressed regions, the diffusion of phosphorus was retarded, and the loops were smaller and sparser. The results of the experiment were qualitatively explained.

CHAPTER VI
SIMULATION OF THE EFFECT OF PATTERNED NITRIDE STRIPES ON POINT AND EXTENDED DEFECTS

The effects of patterned nitride films on the diffusion of phosphorus and the evolution of dislocation loops were experimentally investigated in Chapter V. The diffusion of phosphorus was retarded in regions of compression and enhanced in regions of tension. The dislocation loops were found to be sparser and smaller in regions of compression when compared to the adjacent tensile regions. It was theorized that a compressive pressure field increases the formation energy of an interstitial, thereby reducing their concentrations in those regions. On the other hand, the formation energy of a vacancy decreases in a compressive field. The exact opposite behavior is true in regions of tension. The results of the experiment described in Chapter V were qualitatively explained using these arguments. In this chapter, the models developed in Chapters II, III, and IV are collectively used to quantify the effects observed in Chapter V.

6.1 Simulation of Stress-Assisted Evolution of Dislocation Loops

In Chapter II a model for the evolution of dislocation loops in an inert ambient, based on the Ostwald ripening phenomenon, was developed. The loss or gain of atoms during the anneal was found to be a strong function of loop size. Loops above a certain critical radius gained atoms and grew in size [Equation 2-11]. Loops below the same critical radius lost atoms and eventually dissolved [Equation 2-12]. This loss or gain of atoms for a given loop was also strongly dependent on the concentration of point defects in the bulk at its edge. In the presence of a pressure field the point defect concentrations (Chapter III) are defined as

$$C_I^*(P) = C_I^*(P=0)\exp\left(\frac{-P\Delta V_I}{kT}\right) \tag{6-1}$$

$$C_V^*(P) = C_V^*(P=0)\exp\left(\frac{P\Delta V_V}{kT}\right) \tag{6-2}$$

where $C_{I/V}^*(P)$ is the equilibrium concentration of interstitials/vacancies in the presence of the pressure field, P is the spatially dependent magnitude of the pressure field, k is the Boltzman's constant, and T is the temperature. ΔV_I and ΔV_V are effective interstitial and vacancy expansion volumes, and are defined as

$$\Delta V_I = 1.33\pi\varepsilon r_o^3 \tag{6-3}$$

$$\Delta V_V = 2\pi r_s^2\gamma\Gamma/\mu \tag{6-4}$$

where r_o and ε are defined in Figure 3.7, r_s and Γ are the radius and surface tension of the vacancy well respectively, μ is the shear modulus of silicon, and γ is related to the Poisson's ratio η of the material (=0.3 for silicon) as

$$\gamma = 3.0 \cdot \frac{1-\eta}{1+\eta} \qquad 6\text{-}5$$

The continuity equation for the loss or gain of atoms for a loop with radius R (Equation 2-10) can now be rewritten by including the pressure dependence as

$$\left.\frac{\partial n}{\partial t}\right|_{atRadiusR} = \alpha K_{IL}(C_I(P) - C_{Ib}) - \alpha K_{VL}(C_v(P) - C_{Vb})\big|_{atRadiusR} \qquad 6\text{-}6$$

where α is an effective cross section of the loop layer in the unit of linear length, K_{IL} is the constant of reaction between the interstitials and the dislocation loops, K_{VL} is a similar constant for vacancies, $C_{I/V}(P)$ is the concentration of interstitials/vacancies in the presence of the pressure field, and $C_{Ib/Vb}$ are defined in Equations 2-6 and 2-7.

In presence of a pressure field the equilibrium concentration of point defects would change, altering their concentrations in the bulk, i.e. $C_{I/V}(P)$ is a function of pressure. Thus, Equation 6-6 has an implicit pressure dependence. This implies that the rate of growth of the loops, defined in Equation 2-14, is now spatially dependent, dictated by the pressure field. To illustrate this point, assume that the pressure in a given region is compressive. The quantity on the left in Equation 6-6 would decrease and, therefore, reduce the rate of growth of loops in that region. Similarly, the average rate of growth of loops in a tensile region would increase. This agrees qualitatively with the results of Chapter V. Other loop ensemble properties, such as the maximum and minimum radius, and total loop density, change in accordance with the model described in Chapter II. Since the anneal was done at 900°C, the parameters extracted in Chapter II are used again for the simulations.

6.1.1 Simulation Structure

The structure used in the experiment is pictorially depicted in Figure 5.8. For ease in simulation, the structure shown in Figure 6.1 is used with almost no loss of accuracy. This structure approximates the real structure in the experiment, because the substrate in region A is padded off from the nitride layer by the 300 Å thick oxide layer. The oxide being a viscous material can flow to relieve the compressive stress from the tensile nitride. Simulations were used to confirm this phenomenon. The use of the real structure adds unrealistic noise to the finite element stress simulations in the bulk, as the oxide/nitride/silicon triple point would need an extremely fine grid to sufficiently resolve the edge effect in that region.

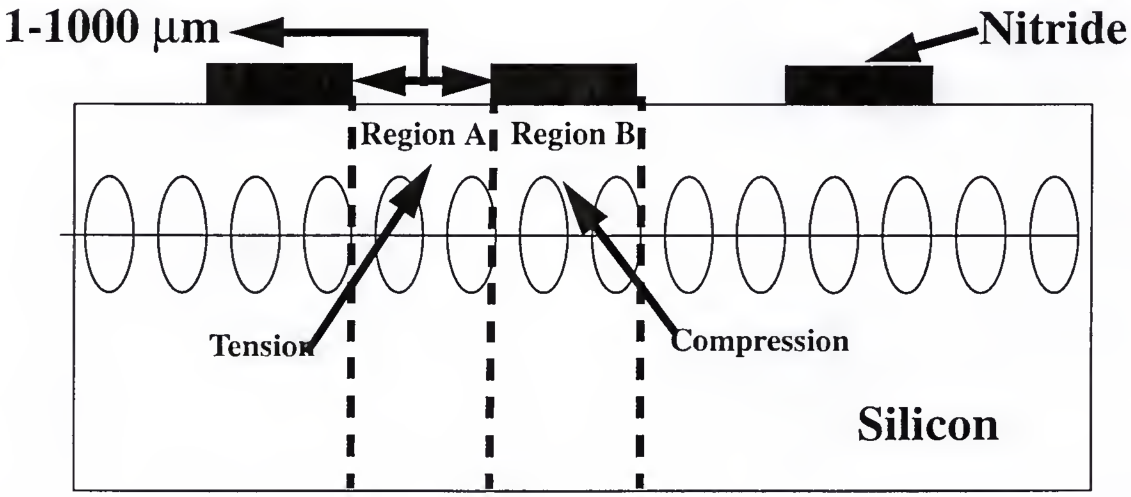


Figure 6.1 Plot illustrating the structure used in FLOOPS to simulate the stress assisted evolution of ion-implanted dislocation loops in silicon. The structure is a good approximation to real structure described in Chapter V.

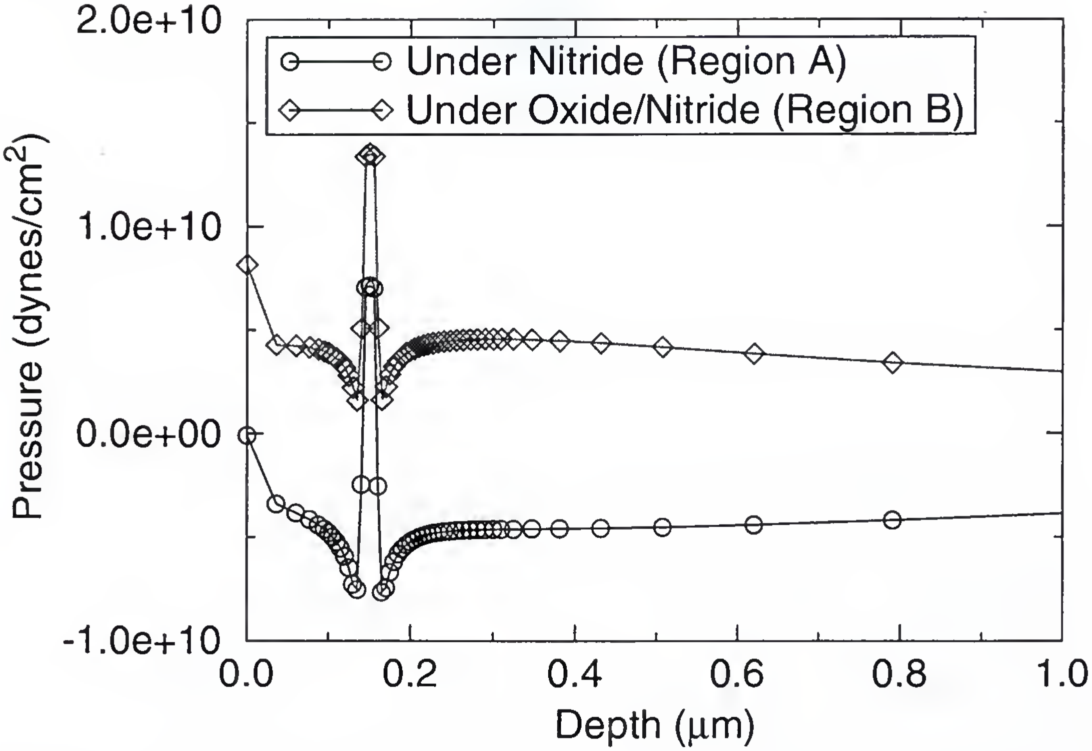


Figure 6.2 Plot of the hydrostatic pressure in the silicon substrate in compressive and tensile regions under the patterned nitride stripes. The dislocation loops can significantly alter the net pressure.

6.1.2 Stress Field in the Substrate

The loops are initialized at a depth of 1500 Å. Multiple nitride stripes are used instead of a single stripe due to reasons explained in Section 4.1.3. It is observed that increasing the number of stripes beyond 3, resulted in almost no improvement in accuracy. An intrinsic stress of 4.0×10^{10} dynes/cm^2 is initialized in the nitride. The stress due to the dislocation loop ensemble is also taken into account based on the models developed in Chapter III. Figure 6.2 shows the variation in the stress as a function of depth in the middle of the two regions (A and B). The dislocation loops can significantly alter the stress field in the silicon substrate in the regions close to the center of the loop layer. The total stress in the bulk is found to be an algebraic superposition of the stress from the nitride stripes and the dislocation loops. Since the average growth rate of the loops is dependent on the stress field near the dislocation layer, this stress must be accounted for while calculating the local point defect concentrations in the bulk.

6.1.3 Point Defect Concentrations in the Bulk

As mentioned earlier, the kinetics of loop evolution are strongly sensitive to point defect concentrations in the bulk. Equations 6-1-6-4 relate the pressure to the equilibrium concentrations of point defects. They are strongly sensitive to ΔV_I and ΔV_V, the effective interstitial and vacancy expansion volumes. Since the interstitials in the case under investigation are "self-interstitials" i.e. silicon atoms themselves, the effective interstitial volume was obtained from Equation 6-3, assuming r_o to be equal to half the radius of single silicon atom. This is an approximation of the exact value, which should be the radius of the cavity into which the "self-interstitial" is inserted. For the vacancy volume, the effective radius r_s, is assumed to be exactly equal to the radius of the missing atom. Thus, the two effective radii are defined as

$$r_s = 2 \times r_o = r_{Si} \qquad \text{6-7}$$

where r_{Si} is the radius of a silicon atom. A dilatation (ε) value of 0.5 was chosen to be consistent with earlier work [38, 56].

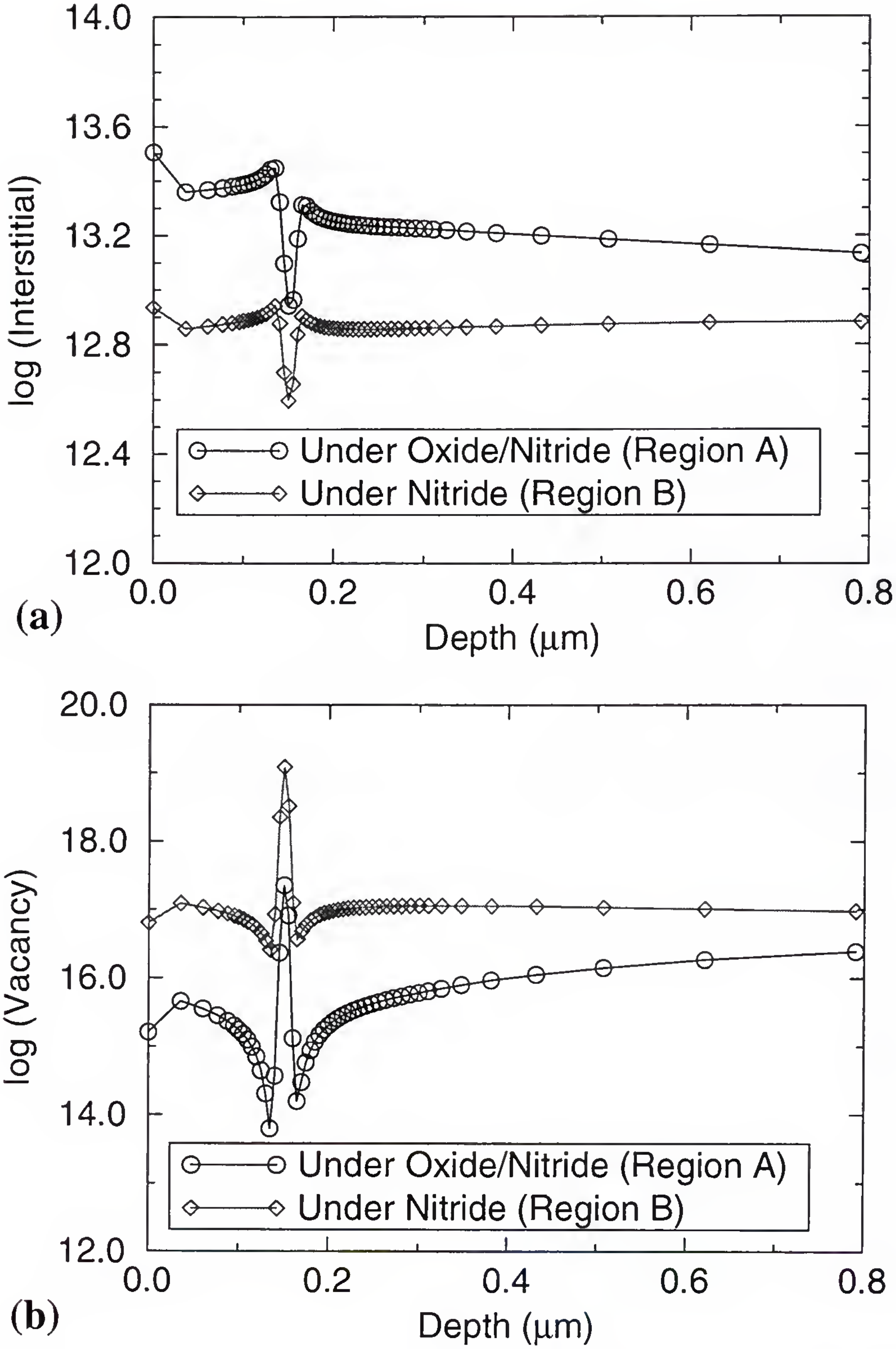


Figure 6.3 A plot of (a) interstitial, and (b) vacancy concentration as a function of depth in response to the pressure plots of Figure 6.2. Note the super/under-saturation of point defect concentrations from their equilibrium values.

6.1.4 Simulation of Average Radius of Loops

Under the conditions of compressive and tensile stress, the point defect concentrations are perturbed from their zero stress values as shown in Figure 6.3. The pressure from the dislocation loop ensemble can significantly perturb the point defect kinetics. The rate of increase in the average radius of the dislocation loops is now spatially dependent, and its time dependence is shown for the case of 4 μm stripes in Figure 6.4. The growth rate, for both regions (A and B), is high in the early stages of the anneal, but saturates after about an hour. The average radius of the loops is higher in the tensile regions (A), as was observed in the experimental data in Chapter V. Thus, the model correctly predicts the trends in the size evolution of the loops.

Simulations were performed to investigate the stripe width dependence of the data seen in Chapter V. The experimental data showed that ΔR_{ave} (Figure 6.4) was a strong function of the stripe width, and decreased with increasing stripe width of the patterned film. Simulations in Chapter IV had suggested that for very small depths into the substrate the stress levels increased with shrinking stripe widths. Since the loops are initialized at a small depth of 1500 Å by the high dose ion-implantation, the loop growth rate should follow this stress dependence. This is reflected in the simulations illustrated in Figure 6.5. The simulated values of ΔR_{ave} are in agreement with the experimental data. For the small stripe widths (1-4 μm), the higher stress levels in the regions close to the film-silicon interface cause a greater under- /super-saturation of point defects in the bulk when compared to the low stress case of the wider stripe width samples. Thus ΔR_{ave} is higher for the smaller stripe widths. The model not only correctly predicts the variation in ΔR_{ave} from the tensile to compressive regions in the same sample, but also brings out its correct stripe width dependence observed in the experimental data. It should be noted that in the simulations ΔR_{ave} was extracted from the middle of the tensile and compressive regions. For example, for the 4 μm stripes, extending from -4.0 to +4.0 microns

$$\Delta R_{ave}(4) = \frac{R_{ave}(2) - R_{ave}(-2)}{R_{ave}(-2)} \tag{6-8}$$

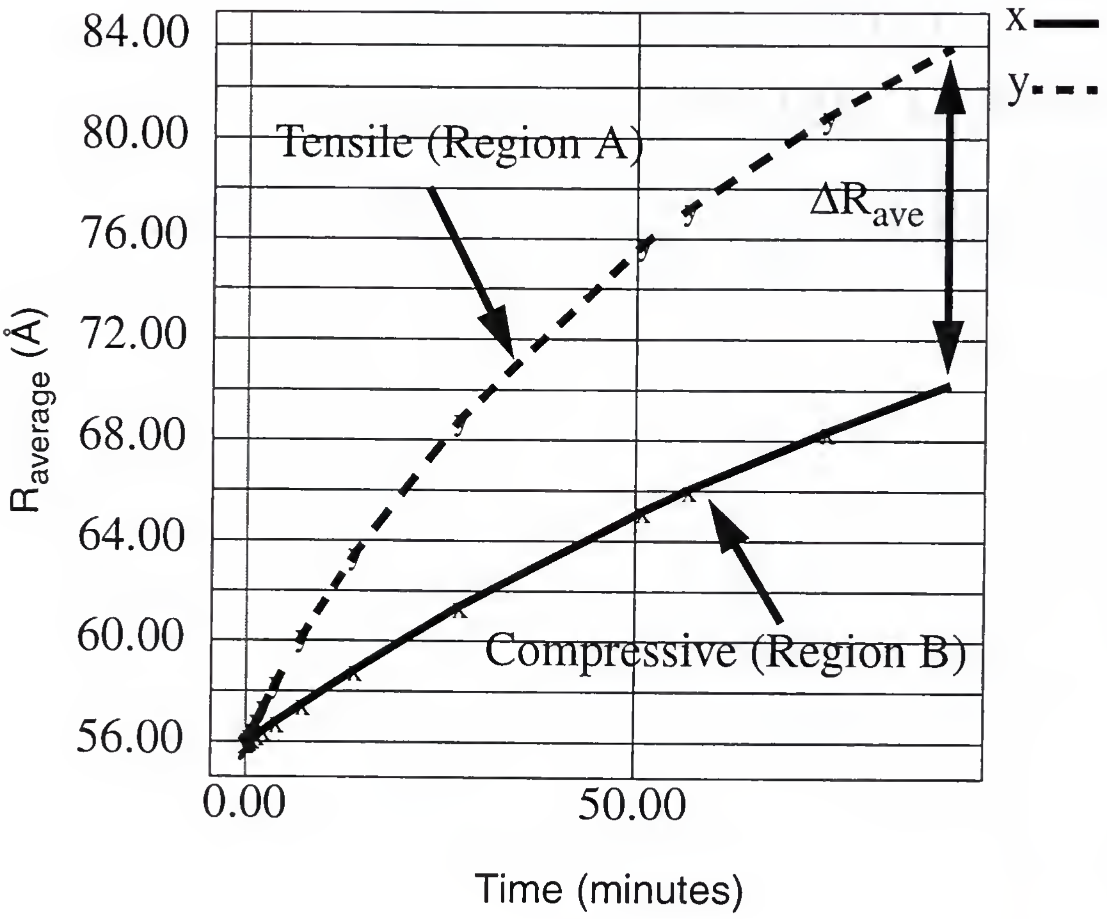


Figure 6.4 A plot of the change in the average radius of the loop ensemble as a function of time in the tensile and compressive regions of substrate for a sample of 4 μm stripe width, and a 1000 Å thick nitride film. The anneal temperature is 900°C.

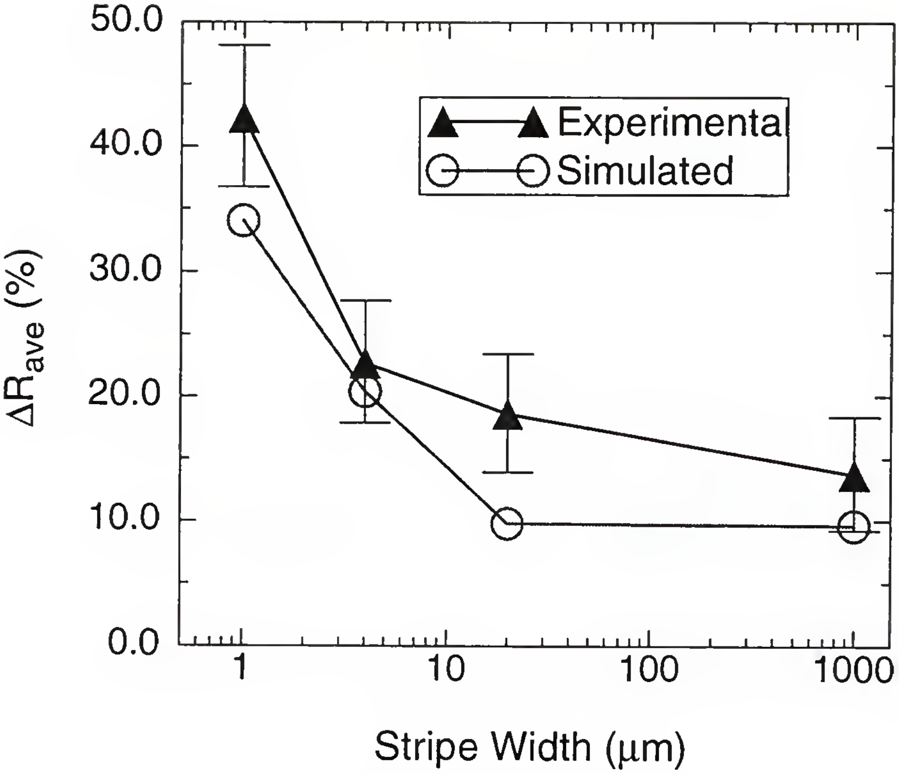


Figure 6.5 Experimental and simulated values of the net change in the average radius of the dislocation loops from the tensile to the compressive regions as a function of stripe-width.

6.1.5 Simulation of the Total Density of Loops

The experimental data in Chapter V indicated that the loops were sparser in the compressive regions of the bulk. The model described in this chapter does not explicitly account for the stress dependence on the total density (D_{all}) of the dislocation loops. Instead, the change in the total density at each time step during the anneal is related to the change in R_{peak} via an empirically extracted parameter [29, Appendix]. The values used for this parameter were consistent with the simulations in Chapter II.

The change in density of the dislocation loops, from the tensile to the compressive regions, was found to be a weak function of the stripe width in the experimental data discussed in Chapter V. The model correctly predicts this weak dependence (Figure 6.6). However, some difference in the magnitudes of ΔD_{all} between the simulation and experiment remain for the larger stripe widths. For the larger stripe widths the error is probably greater than the error-bars plotted, because under plan view TEM it is not possible to count the loops in a region that is exactly in the middle of the stripe. On the other hand the simulations are for differences in the total density of the loops at the middle of the stripes. Larger values of ΔD_{all} were observed in the simulations for regions close to the stripe edges where the stresses are higher.

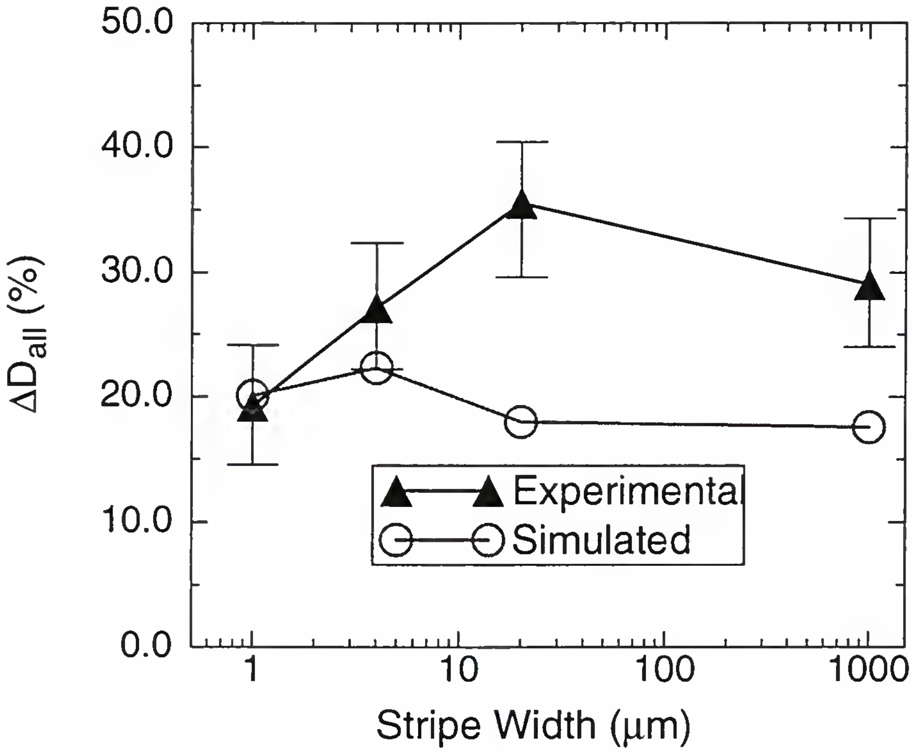


Figure 6.6 Experimental and simulated values of the net change in the total density of the dislocation loops from the tensile to the compressive regions as a function of stripe-width. There is agreement between the simulated and experimental values for the smaller stripe widths. However, for the larger stripe widths some discrepancy is apparent.

6.1.6 Simulation of the Total Number of Captured Atoms

Results of the simulations for the average radius and total density of the dislocation loops were presented in Sections 6.1.5 and 6.1.6 respectively. A quantity of greater interest for process modeling is the total number of trapped interstitials in the dislocation loop ensemble. Loops in regions under compression, which have a large number of vacancies, are more likely to lose a silicon atom to the bulk. Thus, these regions have a smaller number of interstitials trapped in the loops. This was reflected in the experimental data presented in Section 5.2.3. It was observed that ΔN_{trap} decreased with shrinking stripe width. The simulations (Figure 6.7) predict this trend correctly, though for the 20 μm stripe width sample the discrepancy is quite large.

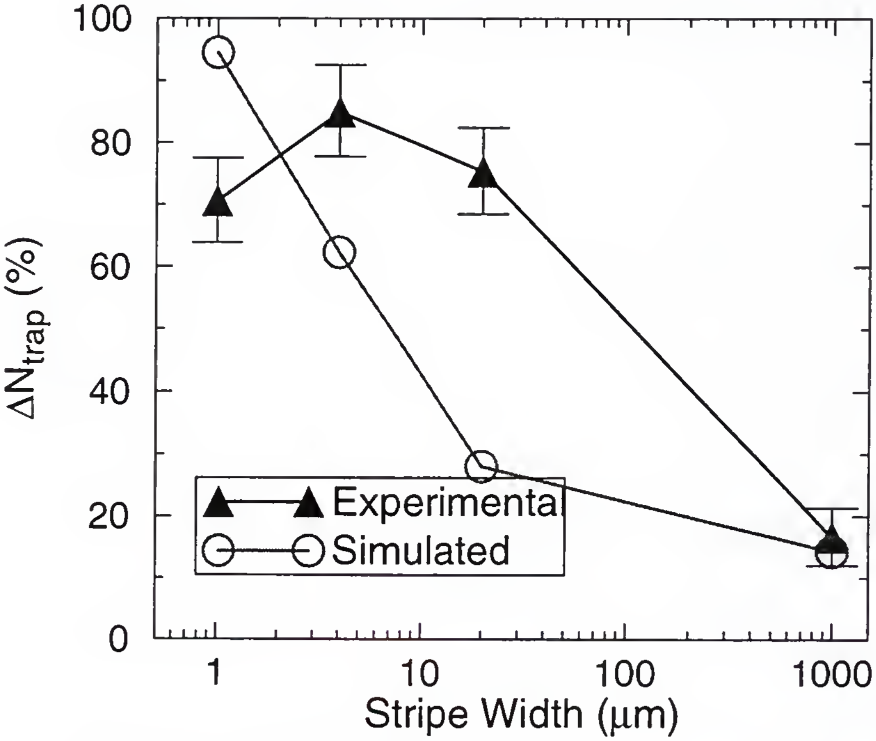


Figure 6.7 Experimental and simulated values of the net change in the total number of trapped interstitials in the dislocation loops from the tensile to the compressive regions as a function of stripe width.

6.2 Simulation of the Stress-Assisted Diffusion of Phosphorus

The effect of a stress field on the local concentration of point defects is described by Equations 6-1 and 6-2. Thus, if a dopant like phosphorus (known to diffuse mainly by an interstitial mechanism) is annealed in the presence of the nitride stripes, it should show a retardation in diffusion in regions of compression. While simulating the stress-assisted diffusion of phosphorus it is also important to incorporate the effect of the stress on the binding energy of the dopant-defect pair. The binding energy of a point defect pair is defined as the difference in the thermodynamic potential of the paired and unpaired point-defect. Physically, the binding energy determines the number of point defect pairs that are present in the bulk. For the zero stress case, the binding energy is a constant dependent only on temperature. For the case when a non-zero stress field exists, the binding energy becomes dependent on the stress at any given location in the substrate. This makes the pairing coefficient a spatially varying quantity; the total number of point defect pairs in equilibrium are written [56] as

$$C^*{}_{AX(P)} \cong C^*{}_{AX(P=0)} \exp\left(\frac{-P\Delta V_{AX}}{kT}\right) \qquad \text{6-9}$$

where P is the hydrostatic pressure, and ΔV_{AX} are the effective volumes for elastic inclusion of dopant-point defect pairs. Mathematically, it is positive for the interstitials and negative for the vacancies. Thus, the equilibrium concentration of phosphorus-interstitial pairs decreases, and phosphorus-vacancy pairs increases in a compressive medium. The model predicts a retardation in the diffusion of phosphorus in a compressive medium. The change in the point defect and dopant-point defect pair concentrations need to be simultaneously accounted for while simulating the stress-assisted diffusion of phosphorus.

The point defect concentration dependence on stress was discussed in Section 6.1.3. Equation 6-9 brings out the effect of a stress field on the dopant-point defect pairs in the substrate and is implemented in FLOOPS by making the pairing coefficient a function of the pressure:

$$K^C_{AX(P)} = K^C_{AX(P=0)}\exp\left(\frac{-P\Delta V_{AX} + P\Delta V_X}{kT}\right) \qquad \text{6-10}$$

where ΔV_{AX} and ΔV_X are positive for interstitials and negative for vacancies. Equation 6-10 implicitly accounts for the physics in Equation 6-9. These equations are strongly sensitive to the effective volumes of the point defect and dopant-point defect pairs.

Under the anneal conditions discussed in Chapter V, simulations showed that the effect of Equations 6-1, 6-2, and 6-10 on the diffusion of phosphorus are comparable. The volumes used for the point defects are the same as described in Section 6.1.3. The value used for ΔV_{PI} is estimated from the radius of a hypothetical sphere with radius equal to the sum of the radii of a phosphorus atom and a silicon self-interstitial. The corresponding volume for a dopant-vacancy pair is more complicated to estimate, and is assumed to be twice that of the dopant-interstitial pair [56]. Since the phosphorus diffuses almost entirely via a vacancy mechanism, the results of the simulations showed a weak dependence on the dopant-vacancy inclusion volumes. The stress levels in the nitride film are modified from Section 6.1.2 to account for the thermal strain at 1000°C.

6.2.1 Simulation Scheme

Once the volumes for the stress-assisted diffusion of phosphorus were defined, a simplified simulation scheme was developed to incorporate the first-order effects discussed in the preceding section. As discussed in Section 6.1.1, a simplified structure (Figure 6.1) approximates the real situation. A chart depicting the simulation scheme is shown in Figure 6.8.

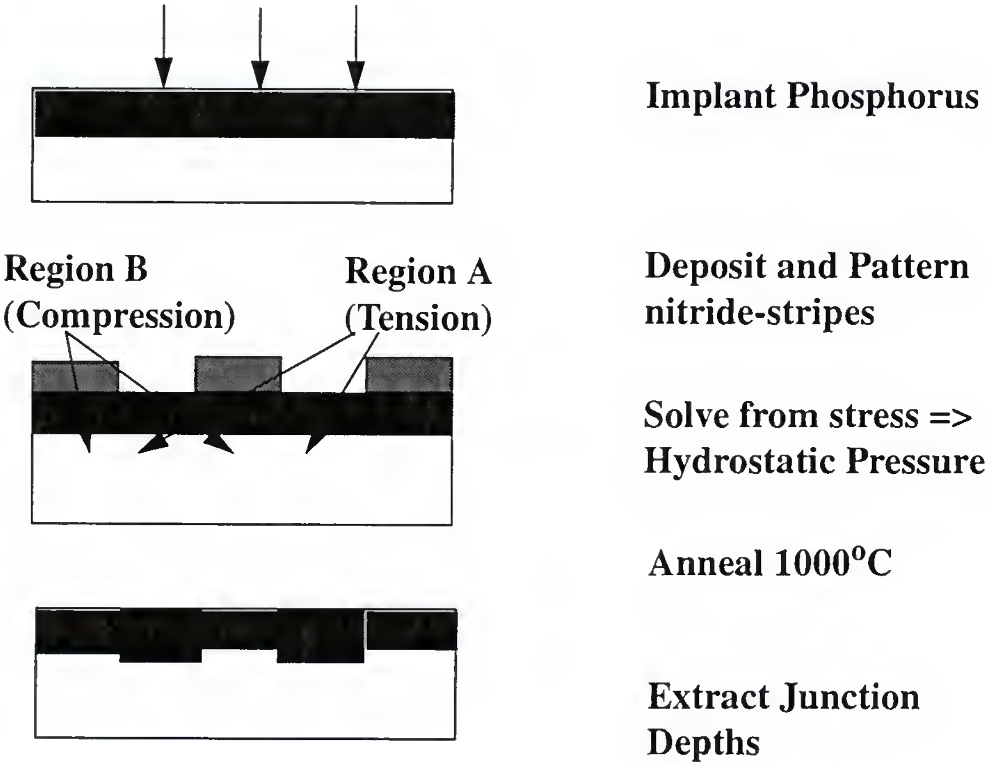


Figure 6.8 Chart depicting the simulation scheme for the stress-assisted diffusion of phosphorus. The anneal in the simulation is carried out after stripping the stripes to eliminate the diffusion dependence of phosphorus on the interface properties.

It should be noted that the anneal is carried out after the stress from the nitride stripes was solved for. To eliminate the differences arising out of the interface properties from region A to B, the stripes are stripped before the anneal (i.e. in the simulation). The stress levels in the substrate are higher in this case than the simulations for the dislocation loops, as the thermal mismatch stress at 1000°C needs to be taken into account. This additional component of stress is absent for the loop simulations, since both the nitride deposition and the anneal were performed at 900°C.

Since the dopant is expected to diffuse to depths of over a micron and the lateral extent of the simulation structure extends to thousands of microns (for the 1000 μm stripes), grid quality is an important issue. Not only is it necessary to resolve junction depths to within hundreds of angstroms, but the accurate estimation of the stress requires fine grid near the nitride stripe edges. For the case of the smaller stripe widths (< 4 μm) the number of grid points was kept within 3500 grid points. For the wider stripe widths maintaining such a grid quality consistently over the entire structure is not possible. To circumvent this problem the grid quality near the nitride stripe edges is maintained, but the grid is coarsened in the middle of the stripes, where the change in the stress or the phosphorus concentration is not rapid. Three nitride stripes are used to mimic the periodicity of the actual structure. The junction depths are extracted form the middle of the structure for both the compressive and tensile regions. The grid density in the vertical direction is maintained at about 50 Å for all the samples simulated. Increasing the grid density beyond this did not result in greater accuracy. Since the net retardations observed in Chapter V were of the order of hundreds of angstroms, such a grid scheme should be adequate.

6.2.2 Simulation Results and Analysis

In this section results from the simulations of the stress-assisted diffusion of phosphorus are presented. The results are compared with the experimental data of Chapter V. Since the diffusion kinetics of phosphorus are strongly dependent on the stress field in the bulk, the stress simulations from patterned nitride stripes described in Chapter IV are used to explain the results. The results indicate a strong coupling between the stress field and point defect and dopant-point defect pair concentrations. The net retardations from compressive to tensile regions are used to benchmark the results. This also facilitates direct comparison of the simulations with experimental data of Chapter V.

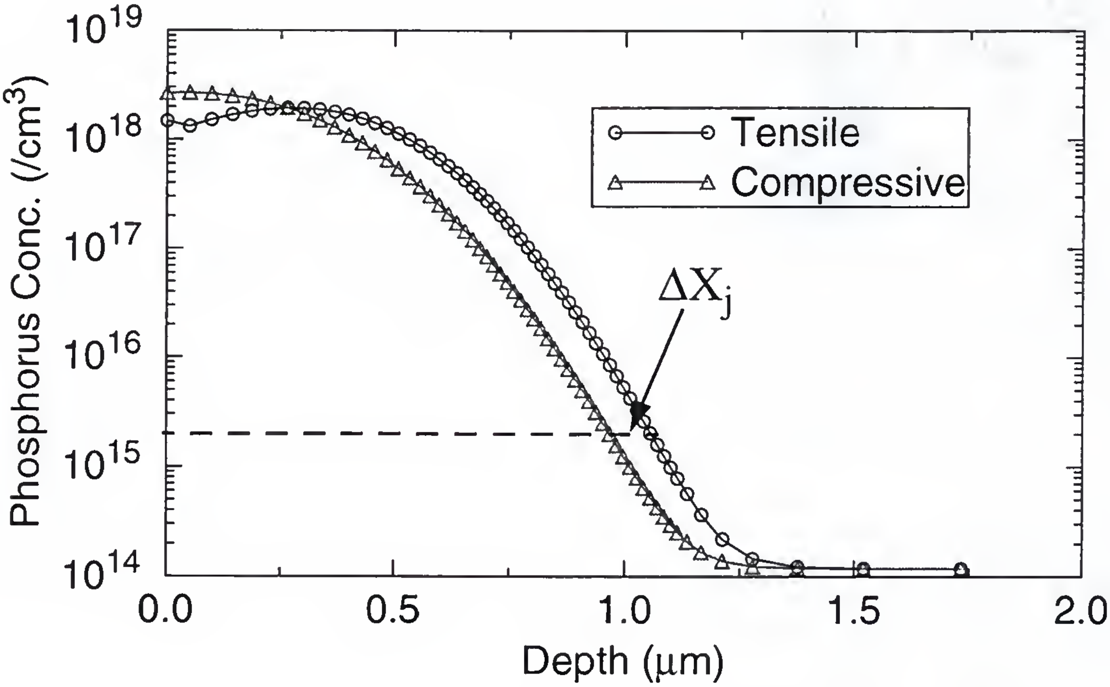


Figure 6.9 Simulated phosphorus concentration profiles in the tensile (Region A) and compressive (Region B) regions of the substrate illustrating the retarded diffusion in the compressed substrate. The simulation is for a 4 μm stripe width, 2000 Å thick nitride film, and for anneal time of 4 hours at 1000°C.

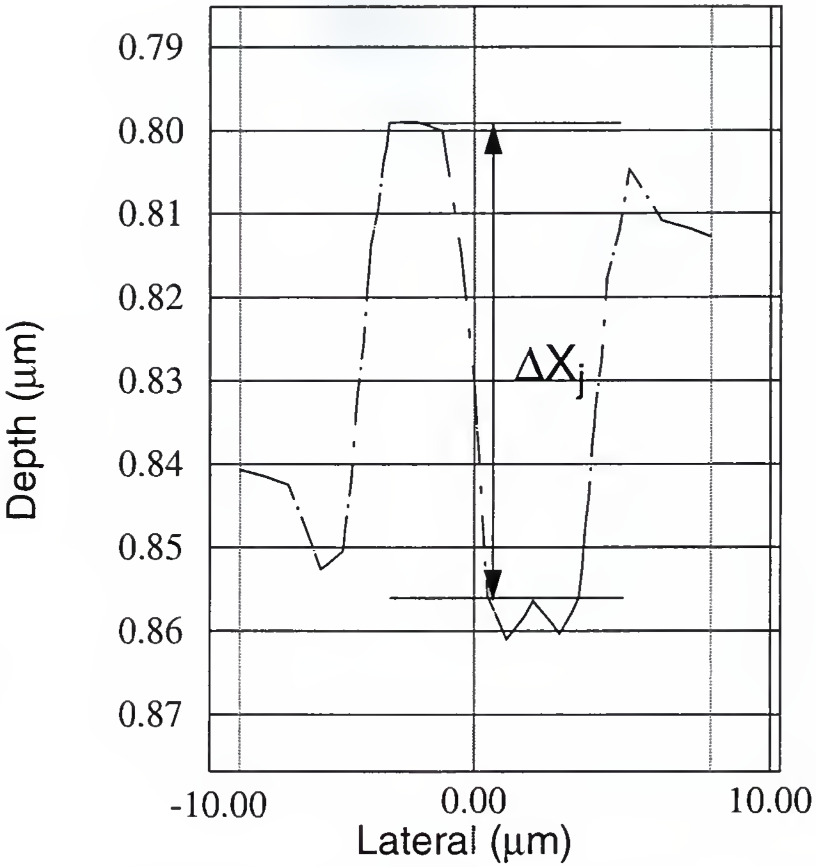


Figure 6.10 A plot of the lateral variation in junction depth for the 4 μm stripe width. It is interesting to note the sharp change in junction depths at the edges of the nitride stripes, where the edge lift-off force is maximum.

For each sample simulated, a net retardation (ΔX_j) from the tensile to the compressive regions is extracted. The concentration at which a junction is defined is chosen as $2x10^{15}/cm^3$. As shown in Figure 6.9, the net retardation (ΔX_j), remains almost constant for phosphorus concentrations below $1x10^{17}/cm^3$ and above $1x10^{15}/cm^3$. This means that when comparing the simulations to the experimental data from junction staining, the error introduced from the junction stain from sample to sample is minimized.

Figure 6.9 illustrates the change in the concentration of phosphorus as a function of depth in the substrate. As expected, the profiles are shallower in the regions where the stripes introduced a compressive stress. The lateral variation in the junction depth for a 4 μm sample is shown in Figure 6.10. The junction depths are a strong function of the local stress. At the edge of the stripes, where the stress changes rapidly from compression to tension, the junction depths follow the stress profile. The net retardations from the junction staining experiment were extracted from the middle of the stripe. This convention is maintained while calculating ΔX_j from the simulations. The sharp peaks seen at the edges of the stripes were not observed in the junction stained samples. This is probably due to the limited lateral resolution of the stained samples. A more sophisticated two-dimensional concentration profiling technique, like the scanning capacitance method, would be needed to experimentally extract these peaks.

The junction depths for the 4 hour anneal are almost a micron into the substrate. For the 2 hour anneal the junction depths are about 0.7 μm. As seen in the experimental data of Chapter V, the net retardation (ΔX_j) is a strong function of the stripe width, and thus the stress in the substrate. The simulations in Chapter IV showed that the stress in the substrate is a strong function of stripe width. For the experimental conditions under investigation, the stress in the shallow regions of the substrate increased with shrinking stripe width. This was directly responsible for the simulation results discussed in Section 6.1, where the stress at shallow depths (< 0.4 μm) governed the dislocation loop kinetics. The stress-assisted diffusion of phosphorus presents a more challenging phenomenon. The diffusion kinetics are now depth dependent, and the stress in both the shallow and deep regions of the substrate will alter the final junction depths. For the deeper regions in the substrate, simulations revealed that the stress increased with an increase of stripe width. The net retardations also followed this trend. After diffusing deeper into the substrate, the dopant kinetics are governed by the stress field in those regions. Thus, the simulation results accurately predict the experimental data.

Figure 6.11 to Figure 6.14 show the simulated values of the net retardation (ΔX_j) compared with the experimental data of Chapter V. The results from the simulations agree with the experimental data. The model accurately predicts the change in the net retardation as a function of the nitride stripe width. The simulations take this into account by not only solving the two-dimensional diffusion equations in FLOOPS, but by also incorporating the stress dependence on the width and thickness of the stripes. The stress determines the local point defect concentrations, while the local dopant concentrations and the stress dependent pairing coefficients determine the number of dopant-point defect pairs available for diffusion.

6.2.3 Validity of Extracted Volumes

The diffusivities of the dopant and point defects used for the simulations are their default values in FLOOPS. The intrinsic stress levels in the nitride film are also the same as in the simulations of Section 6.1, though the additional stress due to the thermal mismatch is added. The effective volumes used for the simulations are consistent with Section 6.1 and Park et al. [56]. Since there is an exponential dependence of the bulk processing variables on these volumes, it is necessary to examine the validity of these parameters with the results of other researchers. This section examines the validity of the model and the methodology for extracting the effective dopant point-defect elastic inclusion volumes.

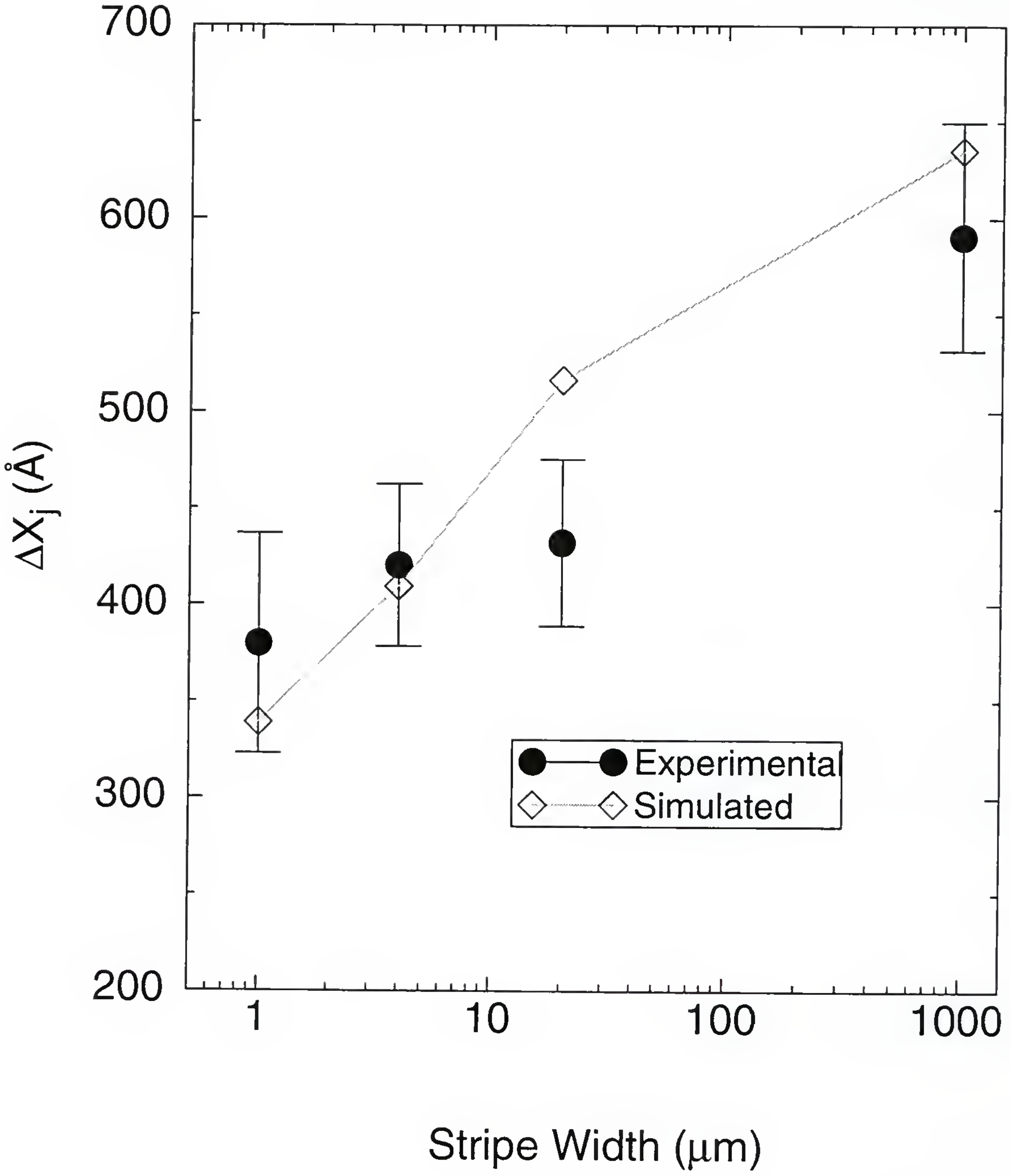


Figure 6.11 Experimental and simulated plots of the net retardation, from the tensile to the compressive regions of the substrate, as a function of stripe width, for a 1000 Å thick nitride film, and a 2 hour anneal at 1000°C. The retardation increases with an increase in stripe width, and is within error-bars (except for the 20 µm stripe width sample).

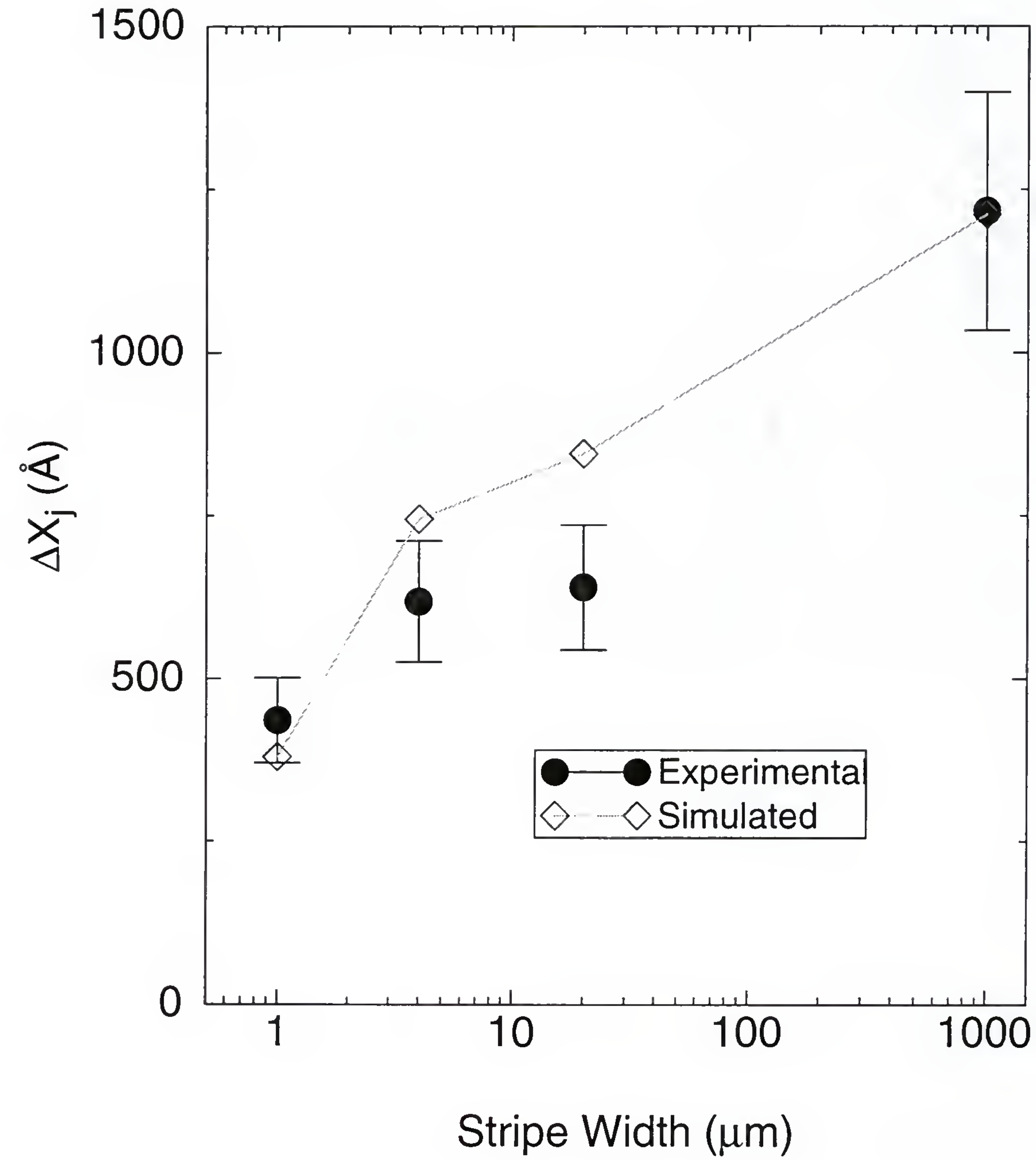


Figure 6.12 Experimental and simulated plots of the net retardation, from the tensile to the compressive regions of the substrate, as a function of stripe width, for a 1000 Å thick nitride film, and a 4 hour anneal at 1000°C. The retardation increases with an increase in stripe width.

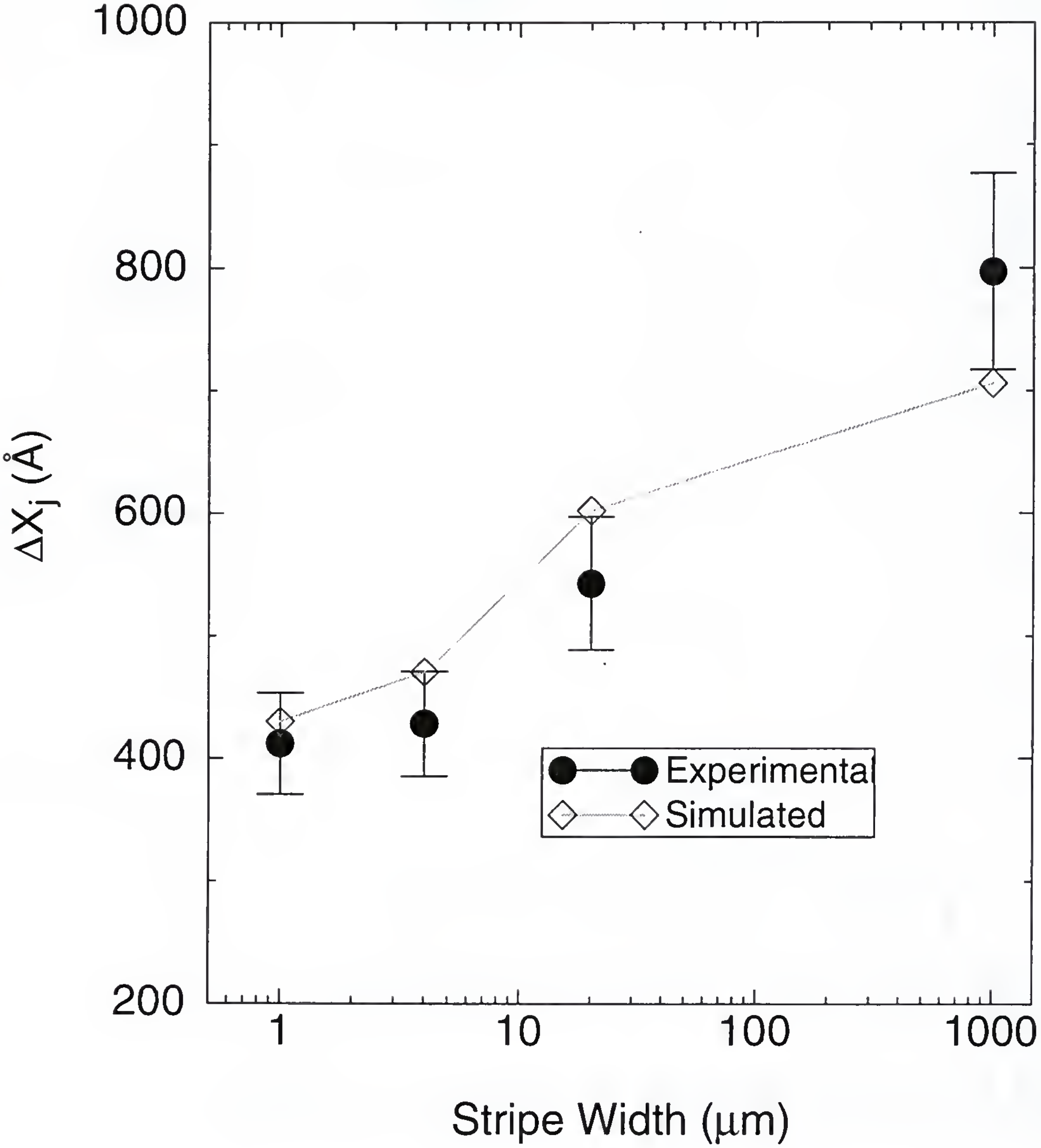


Figure 6.13 Experimental and simulated plots of the net retardation, from the tensile to the compressive regions of the substrate, as a function of stripe width, for a 2000 Å thick nitride film and a 2 hour anneal at 1000°C. The retardation increases with an increase in stripe width.

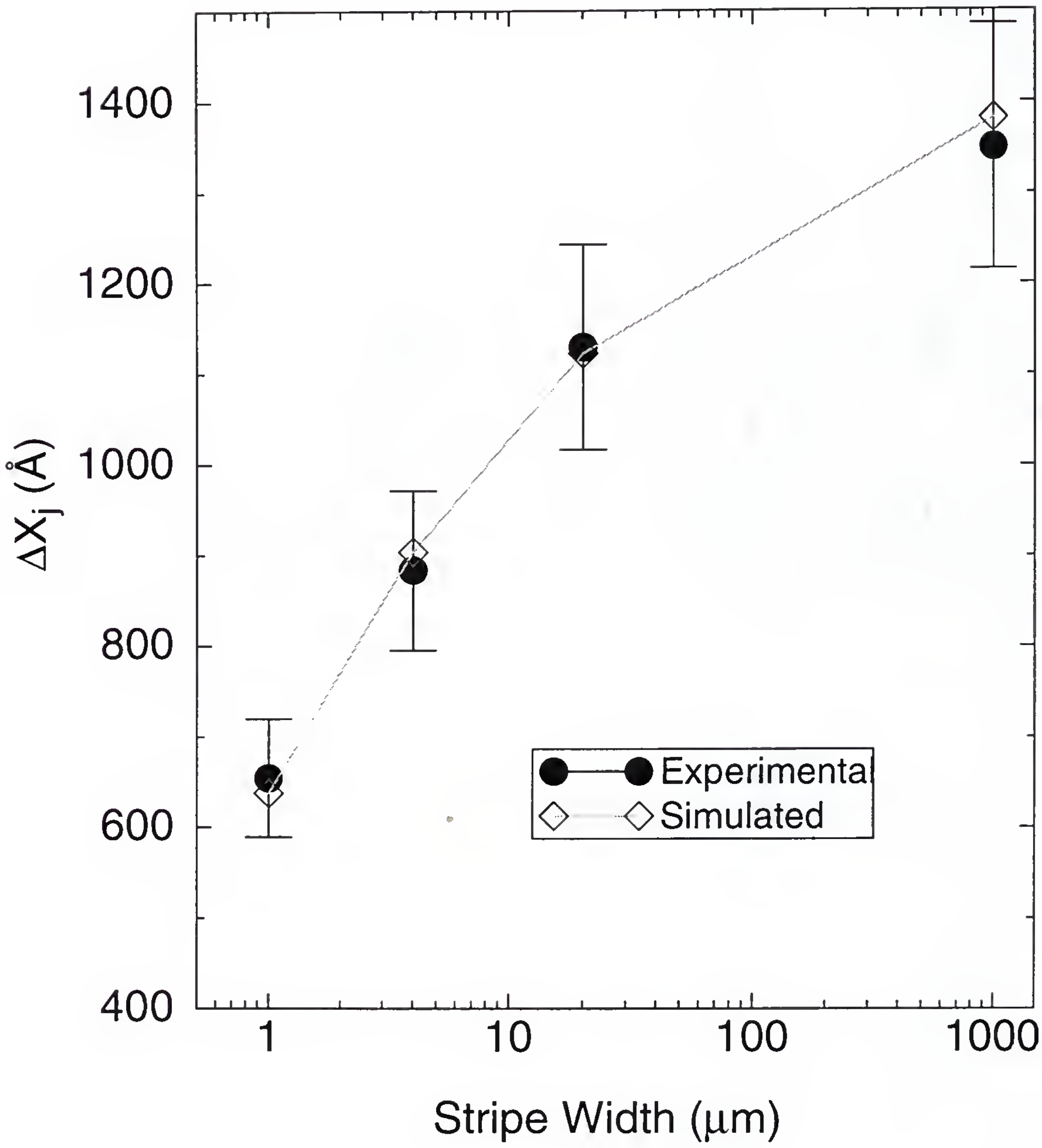


Figure 6.14 Experimental and simulated plots of the net retardation from the tensile to the compressive regions of the substrate, as a function of stripe width, for a 2000 Å thick nitride film and a 4 hour anneal at 1000°C. The retardation increases with an increase in stripe width.

Osada et al. [51] observed retarded diffusion of boron, when annealed under deposited nitride films. They suggested that a tensile stress of ~ 1×10^9 dynes/cm^2 in the film was compressing the silicon below, thereby retarding the diffusion of the dopant. Their test structure was similar to the one presented in Chapter V. Though the effective volumes for the point defects are the same as the ones described in Section 6.1.3, the effective volumes for the dopant-point defect pairs are different for boron. To be consistent with the assumptions made while simulating the stress-assisted diffusion of phosphorus, the value used for ΔV_{BI} is estimated from the radius of a hypothetical sphere with radius equal to the sum of the radii of a boron atom and a silicon self-interstitial. The corresponding volume for a boron-vacancy pair is assumed, as before, to be twice that of the dopant-interstitial pair ($\Delta V_{BV} = 2 \times \Delta V_{BI}$).

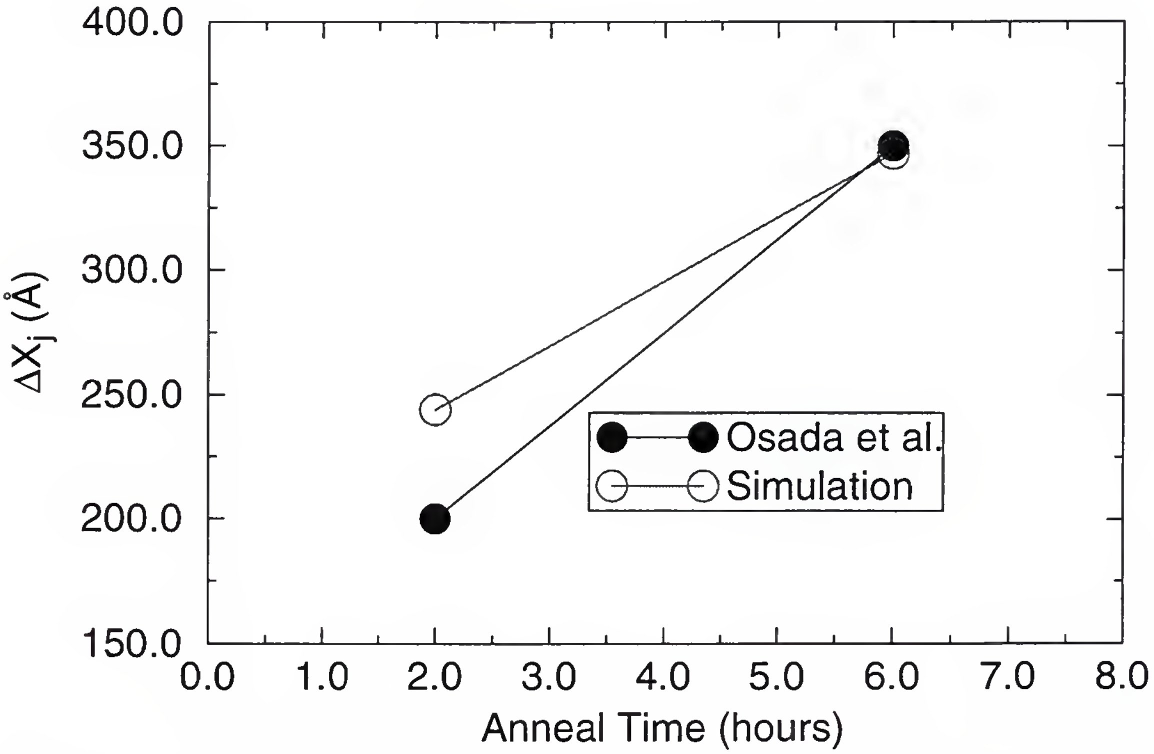


Figure 6.15 Net retardation in diffusion (at 1014°C), due to compressive stress in the substrate, for a 7.5×10^{13}/cm^2, 70 keV boron implant. The simulation is compared with data from Osada et al. [51].

The results of the simulations are shown in Figure 6.15. The implanted dopant is boron (70 keV, $7.5\mathrm{x}10^{13}/\mathrm{cm}^2$) and the anneal is performed at 1014°C for 2 and 6 hours. The net retardation from the simulations matches well with the data from Osada et al. [51]. The experimental data indicates the absence of relaxation in the stress in silicon with time. This is probably because a major component of the stress is due to the thermal mismatch between the nitride and silicon substrate. This stress is present as long as the anneal temperature is maintained at 1014°C.

Manda [57] investigated the effect of uniaxial stress on the diffusion of boron and arsenic in silicon. Instead of using patterned films to introduce stress in the substrate, an in-situ three point bending arrangement was used to introduce a uniaxial mechanical stress in the sample. Low dose boron ($1\mathrm{x}10^{13}/\mathrm{cm}^2$, 100 keV) was annealed at various time and temperatures. The loading configurations were such that the peak stress in the middle of the sample was between $1\mathrm{x}10^8$ and $3\mathrm{x}10^8$ dynes/cm^2. The stress decayed linearly towards the lateral edges of the samples. The results showed no observable effects on the diffusion of the dopants. The work could be significant in extracting the upper bounds for the effective volumes, as the stress levels in the silicon are accurately known from the loading conditions.

It should be mentioned here that the lack of an observable retardation for boron, or an enhancement for arsenic could also be due to the uniaxial nature of the stress, though there is no reason or experimental data to support this hypothesis. The models described in this chapter do not account for the uniaxial nature of the stress. The important quantity is the hydrostatic pressure P, which is the average of the vertical and lateral components of the stress tensor, i.e.

$$P = \frac{\sigma_{xx} + \sigma_{yy}}{2} \qquad 6\text{-}11$$

where the two-dimensional simulation is in the x-y plane, σ_{xx} and σ_{yy} are the normal components of the stress in the vertical and lateral directions, respectively. The simulations thus treat the uniaxial stress in the substrate with

$$\sigma_{yy} = 0.0 \qquad 6\text{-}12$$

and

$$P = \frac{\sigma_{xx}}{2.0} \qquad 6\text{-}13$$

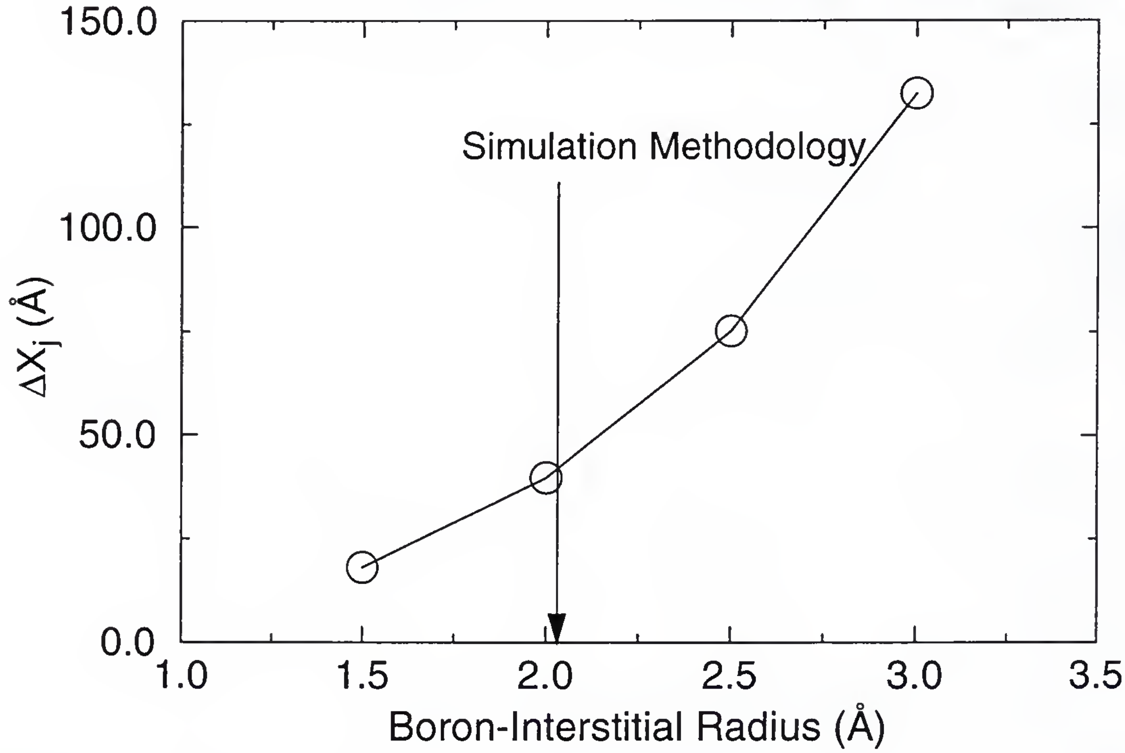


Figure 6.16 Net enhancements in boron diffusion due to tensile stress as a function of the radius of the dopant-interstitial pair. Note the absence of any enhancement for radii equal or less than what was used in the simulation scheme throughout this chapter. The corresponding radii for the boron-vacancy pair are double that of the boron-interstitial pair.

Figure 6.16 shows the simulated net enhancements in the diffusion of boron due to the tensile loading conditions in the wafer. It can be seen that under such levels of stress and the dopant-defect volumes described earlier there is no observable effect on the diffusion of boron. The net enhancements are below 50 Å and are at the resolution limit of profiling methods such as SIMS. However, if the elastic inclusion radii of the dopant-defect pairs are increased beyond what has been used consistently throughout this chapter, a marked increase in enhancement of boron is observed. Therefore, the radii used in this chapter form an upper bound to this parameter.

6.3 Effect of Stress on Device Characteristics

The experimental results of Chapter V and the simulations of this chapter suggest that stress of the order of 1.0-5.0x10^9 dynes/cm^2 can significantly alter the kinetics of dopant diffusion. Since device properties are strongly sensitive to the dopant profiles in the bulk, it is useful to investigate the effect of stress-assisted diffusion on device characteristics. In particular, the effect of stress in the channel of a MOSFET is investigated.

Figure 6.17 shows the diffused profiles under various stress conditions in the channel. The stress levels in the channel are representative of the real stress in a MOSFET of a modern process. Under these conditions, the net charge close to the gate-oxide/silicon interface is maximum for the compressed substrate. Devices under tension exhibited the maximum diffusion, causing the net charge in the depletion region of the MOSFET to be reduced. This modulation in the magnitude of the charge is responsible for altering the device characteristics discussed below. It should be noted that the simulations do not account for the effect of strain on the bandgap in the semiconductor.

The diffused profiles were fed into the device simulator MEDICI [58]. The drain current versus gate voltage characteristics for 0.5 Volt drain bias were extracted for the three profiles. The results of the MEDICI simulations are shown in Figure 6.18. The results show that the stress can significantly affect device properties such as threshold voltage and sub-threshold slopes. Since the simulations are on a representative device, the trends instead of the actual magnitudes of the device properties are discussed. Due to the extra charge near the oxide/silicon interface in the compressed substrate the threshold voltage is higher for these devices. The threshold voltage for the samples in tension are ~ 30% lower than the compressed devices. For low voltages devices the differences are significant.

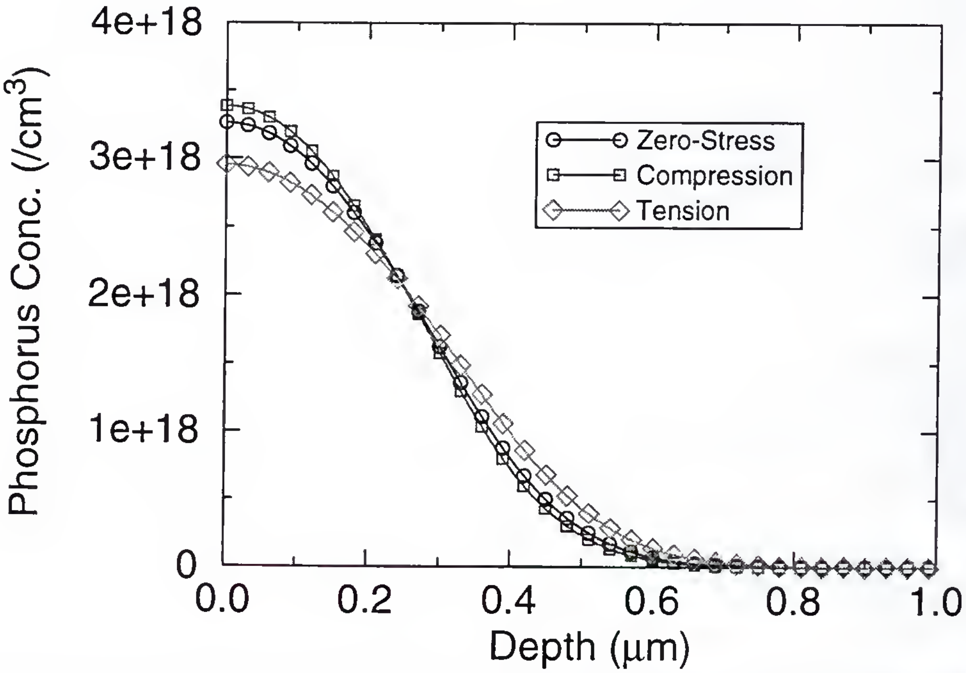


Figure 6.17 Dopant profiles as a function of stress in the channel region of a MOSFET. The compressed channels have a larger charge in regions close to the oxide/silicon interface.

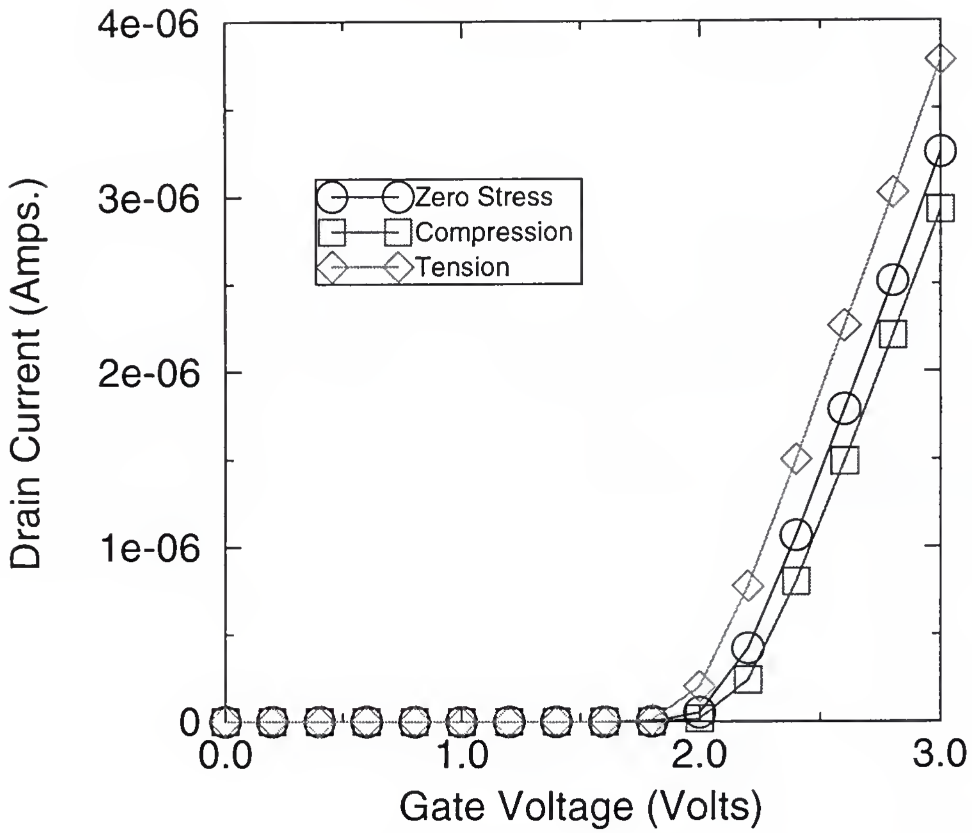


Figure 6.18 The drain current versus voltage characteristics for devices with channel profiles shown in Figure 6.17. The threshold voltage is maximum for the devices in compression.

6.4 Summary

A simulation methodology is developed for predicting the stress-assisted diffusion of dopants, and the stress-assisted evolution of dislocation loops. The experimental data from Chapter V is used to verify the validity of this scheme. Upper bounds for point-defect and dopant-point defect elastic volumes are extracted. Using these volumes the results of other researchers are simulated and the validity of the model verified.

CHAPTER VII
SUMMARY, CONCLUSIONS, AND RECOMMENDATIONS FOR FUTURE WORK

7.1 Summary

In this dissertation, some of the important sources of stress in ULSI technology have been analyzed and modeled. Based on the balance of forces principle, the finite element code in FLOOPS was used to develop models for a variety of sources of crystal strain. The models allow for two-dimensional, and in some instances three-dimensional simulation of stress in the silicon substrate. The predictive capability of the models was verified with experimental data for most cases. A methodology was developed in each instance, to illustrate their use in the field of IC-TCAD. Furthermore, their use as tools for optimizing existing technologies or developing new ones was illustrated.

In Chapter I, an extensive survey of the existing literature on the subject was presented. The sources of stress were classified into five categories. A brief description about each source followed by their implications on technology was presented. Based on the current understanding of the issues it was decided to investigate three different source of stress; ion-implanted dislocation loops, thin films, and epitaxial films. Motivations for studying each of the stress producing categories were presented.

The stress from dislocation loops was found to be strongly sensitive to the loop ensemble size and density. Since these were a function of the anneal conditions, a model for the evolution of dislocation loops in an inert ambient was developed in Chapter II. The model was based on the Ostwald ripening phenomenon, where the bigger loops grew at the expense of the smaller ones. A critical radius, which defined the boundary between the "smaller" and "bigger" loops, was identified. Based on the critical radius, the model calculated the flux of interstitial atoms moving from the smaller to the larger loops, which represented an increase in their size. This coarsening of loops was most evident at temperatures in the 800°C to 900°C range. In this temperature range the total number of trapped atoms in the loops remained almost constant with anneal time. The rate of growth of loops at low temperatures (~700°C) was found to be small. For anneals at high temperatures (1000°C), the loops were in a dissolution regime, showing a sharp increase in the average radius and sharp fall in the total density of the ensemble. The model correctly predicted the slow growth rate at 700°C, the coarsening in the 800°C to 900°C range, and the dissolution at 1000°C. Parameters defining the magnitude of interaction between the interstitials and the dislocation loop ensemble were extracted for the 700-1000°C temperature range.

A model to estimate the stress distribution in the substrate from a dislocation loop ensemble was developed in Chapter III. It was based on the number of excess silicon atoms (interstitials) that were trapped in the loops. This depth dependent quantity was divided by the atomic density of silicon to represent a net intrinsic strain in the lattice. Using this as an initial strain force in the structure, the finite element code solved for the resultant stress in the lattice. The stress was found to be strongly sensitive to the size and distribution of the loops. Therefore, the loop evolution model of Chapter II was used in conjunction with the stress model to predict the change in stress with anneal time. The correlation between the loop ensemble properties and the strain in the lattice was explained. In particular, the peak value of the strain in the lattice was found to be strongly dependent on the total number of silicon atoms trapped in the dislocation loop ensemble. The peak stress in the substrate was experimentally obtained from x-ray rocking curve analysis, and was used to verify the validity of the model. For most anneal conditions, results from the simulations were consistent with the experimental data. In addition to providing the magnitudes of the peak stress, the simulations predicted the spatial variation of the stress in the lattice. The tension at the loop layer edges was found to be strongly sensitive to the boundary condition for the displacement vector at the lateral edges of the structure. By allowing the structure to deform laterally, a larger tension was observed at the edges of the loops. This was in accordance with the analytical solutions of loop stress.

In Chapter IV, models for the stress in the silicon substrate from overlying films were developed. It was shown that the stress in the substrate increases several fold, once a continuous film is patterned into a series of multiple stripes. For patterned films, the stress in the substrate was found to be a sum of the mask "edge" force and the direct film stress. It was observed that the stress from adjacent stripes cannot be neglected while solving for the stress under a stripe. The ratio of film width to thickness was shown to be critical in determining the profile of the resultant stress in the substrate. For a ratio of ~ 8 the lateral stress profile in the middle of the stripe was flat in regions close to the film/silicon interface. The models developed in this chapter were used in Chapter V for the design of the experiment, and subsequently in Chapter VI to predict the effect of stress on bulk processing variables.

Models for wafer bow due to lattice mismatched epitaxial films were also developed in Chapter IV. This involved the use of a new boundary condition, where the lateral and the bottom edges of the simulation structure are allowed to deform in both directions of the simulation plane. A single point in the middle of the bottom edge of the structure was restricted to zero displacement to prevent rigid body motion. It was observed that the wafer bow increased when the magnitude of the mismatch between the epitaxial film and the silicon substrate was increased. The bow was also shown to be directly proportional to the thickness of the epitaxial film. A simulation scheme to predict the effects of a technique called "compensation" was developed. This facilitated the optimization of the technique for minimum wafer bow.

An experimental procedure was designed to investigate the effect of patterned nitride stripes on the diffusion of phosphorus and evolution of ion-implanted dislocation loops in Chapter V. It was observed that the diffusion of phosphorus was retarded in regions where the overlying nitride film was in direct contact with the substrate (i.e. in regions of compression). On the other hand, regions of tension showed a net enhancement in the diffusion of the dopant. The net retardations/enhancements were sensitive to the width and thickness of the nitride stripes. They increased with increasing film thickness or stripe width. The evolution of dislocation loops was also shown to be spatially dependent under the patterned stripes. Under plan view TEM, it was observed that the dislocation loops were smaller and sparser in regions of compression when compared to their distribution characteristics in regions of tension. The difference in the number of trapped interstitials from the tensed to the compressed regions of the substrate was the most for the smallest stripe width samples.

A simulation methodology, based on the models of Chapters II, III, and IV, and the experimental results of Chapter V, was developed in Chapter VI. The stress in the silicon substrate from a series of patterned nitride stripes was obtained from the models developed in this chapter. Using these values, the effects of stress on point defect concentrations were incorporated using the loop evolution models of Chapter II. The simulation scheme accurately predicted the stress-assisted evolution of dislocation loops.

The effect of stress on the concentration of dopant-defect pairs was incorporated by making the pairing coefficient exponentially dependent on the magnitude of the local hydrostatic pressure. The results of the diffusion simulations were in agreement with the experimental data of Chapter V. The extracted inclusion volumes for point defects and dopant-point defect pairs were used to simulate the experiments of other researchers. Again, an agreement between the simulated and experimental data was obtained. Based on these results an upper bound for the volumes used was extracted.

7.2 Conclusions and Recommendations for Future Work

Some of the important sources of stress in ULSI technology have been analyzed and modeled as part of this dissertation. The emphasis has been to develop predictive models or simulation schemes, which could be used as optimization tools by engineers working on alleviating such problems. In addition, the critical levels of stress have been identified. Such information can be used to determine when stress levels in the substrate need to be taken into account while designing a new process.

The models developed in Chapter II predict the time evolution of dislocation loops in an inert ambient. They require the initialization of the size and density of the loop distribution as an input. The size and density of the dislocation loop ensemble depend on the implant energy and dose. Therefore, a predictive model which incorporates the nucleation aspects of the dislocation loops is needed as an input to this work. This would involve an extensive experimental characterization of the nucleation kinetics of type-II dislocation loops. The model should taken into account the dose, energy, and species dependencies.

Recent studies have shown that <311> defects play an important role in Transient Enhanced Diffusion (TED) kinetics [59-61]. Unlike the circular shape of the dislocation loops, these extended defects are rod shaped. However, the annealing kinetics of these defects are qualitatively similar to that of the dislocation loops described in Chapter II. They are formed from the initial implant damage, and grow or dissolve by the absorption or emission of point defects; just like the dislocation loops. A model for their evolution has been developed by Law and Jones [62]. Further calibration for this modeling approach to investigate species and dose dependence of the implant is recommended. Also, models which predict the nucleation of these extended defects would be useful.

In Chapter III, the models for crystal strain provide the user with a means of predicting the stress levels in the substrate from a dislocation loop ensemble. The current status of research and results is satisfactory, as the model is in agreement with the experimental data and the analytical techniques of Park, Jones, and Law [29].

Any defect, whether point, extended, or dopant, is a source of strain in the silicon lattice. Therefore, it is recommended that other sources of stress such as point defects and <311> defects should be part of a complete stress modeling methodology. For point defects, an approach based on the number of extra silicon atoms in the lattice (Chapter III) should suffice. This modeling approach could be extended for calculating stress from high dopant concentrations or dopant precipitates. However, for modeling stress effects from the <311> defects a more complex scheme is needed because of the rod like nature of the defects.

Models for stress from patterned and continuous films described in Chapter IV are adequate for most static stress calculations. The model has been extended to three dimensions, though the results from these simulations are not presented as they are beyond the scope of this dissertation. The models for stress and wafer bow from epitaxial films should be sufficient for optimizing the wafer bow problems in 8 inch wafers.

More experimental data is needed to investigate stress from isolation trenches. Due to the complex shape of some of these structures the simulation results are grid dependent. For greater accuracy the finite element solution of stress would have to be obtained for the entire (silicon and trench-fill) structure. This would enormously increase the computation time. Therefore, a more thorough simulation scheme is needed while solving for stress from these structures. In addition, it would be useful to develop a scheme to investigate stress in the silicon substrates due to LOCOS structures. Some of these schemes are currently under investigation by several researchers [63].

The experimental results of Chapter V are the first evidence of dislocation loop evolution disparity between compressed and tensed regions of the substrate. The loops are found to be sparser and smaller in regions of compression when compared to the tensed regions. As mentioned earlier in this chapter, <311> defect evolution is known to strongly govern diffusion kinetics. Therefore, it would be useful to experimentally investigate the effect of stress on <311> defect evolution.

An inadequacy in the results of the dislocation loop experiment is that under plan view TEM, it is not possible to confirm whether the area under investigation is directly under the nitride film (compressed) or under the nitride/oxide composite (tensed). In this experiment, the results from the wide (1000 μm) stripe width samples, where it was possible to prepare different samples for the compressed and tensed regions, were extrapolated for the smaller stripe width samples to predict that sparser and smaller loops were consistently under the nitride, i.e. in compression.

The results of the experimental investigations of Chapter V also show that stress levels above $1x10^9$ dynes/cm^2 can alter the diffusion kinetics of dopants. The experimental data from this study and the work of other researchers is proof of the importance of incorporating stress dependent diffusion models into process simulators.

A major challenge while designing the experiment of Chapter V was to introduce a known stress in the silicon substrate. As was shown by the simulations of Chapter IV, introducing stress from a series of nitride stripes is useful because it introduces compression and tension simultaneously. However, the magnitude of the stress is strongly sensitive to the film width, thickness or deposition conditions. Therefore, it is recommended that before designing any future experiments for investigating stress-assisted phenomenon in the bulk, the stress profiles be determined from simulations and/or experiment. Another source of stress are continuous films. The stress from these films is much less than their equivalent patterned films. However, the deposition conditions could be tailored to introduce sufficient stress in the substrate. The use of the 3-point in-situ loading technique was demonstrated by Manda [57]. It is a useful method of introducing stress in the silicon substrate, though the logistics of setting up a loading system in a furnace could prove expensive and time consuming.

The simulation scheme of Chapter VI to predict the effect of stress on dislocation loop evolution and the diffusion of phosphorus is a useful method for simulating stress related effects in the bulk. The volumes extracted should form an upper bound to their actual values. Though the results of the simulations match well with the experimental data, better calibration of the models can be obtained from SIMS analysis of the diffusion profiles.

With the continued shrinkage of device dimensions computationaly efficient models and simulation methodologies for predicting stress levels in the bulk are becoming essential for optimum device and process design. Some of the work in this regard is already in progress. It is hoped that this work will form the basis of further development of stress prediction models in process simulators like FLOOPS.

APPENDIX

This appendix describes the parameters extracted in the various chapters of this dissertation.

Chapter II:

The constant of interaction between interstitials and dislocation loops:

$$K_{IL} = 1.6x10^{7}\exp(-1.01/kT)$$

The constant of interaction between vacancies and dislocation loops:

$$K_{VL} = 0.0$$

The effective capture cross-section (cm):

$$\alpha = 7.5 \times 10^{-7}$$

The change in $L_{tot} = (0.5/\sqrt{D_{tot}})$, where D_{tot} is the total density, as a function of the average radius of the loop ensemble $R_{ave} = (R_{min} + R_{peak} + R_{max})/3.0$:

$$\frac{dL_{tot}}{dR_{ave}} = 1 \times 10^{3}\exp\left(\frac{0.494}{kT}\right)$$

The change in the maximum and minimum radius as a function of the peak radius:

$$\frac{dR_{max}}{dR_{peak}} = 1.0, \frac{dR_{min}}{dR_{peak}} = 0.0$$

Chapter III:

The dilatation:

$\varepsilon = 0.5$

The elastic inclusion radii for interstitials (r_o), and vacancies (r_s) in centimeters:

$r_o = 1.15 \times 10^{-8}$, $r_s = 2.3 \times 10^{-8}$

Chapter IV:

Material Flow Constants for *silicon*:

Poisson's ratio (ν) = 0.3;

Young's Modulus (Y_m) = $1.7\text{x}10^{12}$ dynes/cm^2;

Viscosity (η) = $1\text{x}10^{20}$ Po.

Material Flow Constants for *silicon nitride*:

Poisson's ratio (ν) = 0.29;

Young's Modulus (Y_m) = $3.89\text{x}10^{12}$ dynes/cm^2;

Viscosity (η) = $1\text{x}10^{20}$ Po.

Chapter VI:

Dilatation and elastic inclusion radii for point defects as in Chapter III.

Material flow constants for silicon and silicon nitride as in Chapter IV.

Dilatation and elastic inclusion radii for dopant-point defect pairs as described in Chapter VI.

REFERENCES

1 W. Fichtner, L. W. Nagel, B. R. Penumalli, W. P. Peterson, and J. L. D'Arcy, "The Impact of Supercomputers on IC Technology; Development and Design," *Proc. IEEE*, **72**, p. 96 (1984).

2. S. M. Hu, "Temperature Distribution and Stresses in Circular Wafers in a Row During Radiative Cooling," *J. Appl. Phys.*, **40**, p. 4413 (1969).

3. B. J. Van Schravendijk, W. L De Koning, and W. C. Nuijen, "Modeling and Control of the Wafer Temperatures in a Diffusion Furnace," *J. Appl. Phys.*, **61** (4), p. 1620 (1987).

4. M. A. Tavel and E. W. Hearn, "An Interactive Simulation of Heating and Cooling a Row of Silicon Wafers," *J. Electrochem. Soc.*, **135**, p. 1266 (1988).

5. S. Yamagishi, "Anticlastic Bending Silicon Wafers Induced during Thermal Cycling," *Jpn. J. of Appl. Phys.*, **12**, p. 1748 (1973).

6. H. C. Liu and S. P. Murarka, "Elastic and Viscoelastic Analysis of Stress in Thin Films," *J. Appl. Phys.*, **72** (8), p. 3458 (1992).

7. Y. Hayafuji, T. Shimada, and S. Kawado, "Dislocation Configuration under Periodic Stress Field Caused by a Poly-Silicon Film on Silicon," in *Semiconductor Silicon*, Edited by H. R. Huff and E. Sirtl (Electrochemical Society, Pennington, NJ, 1977), p. 750.

8. S. Isomae, Y. Tamaki, A. Yajima, M. Nanba, and M. Maki, "Dislocation Generation at Si_3N_4 Film Edges on Silicon Substrates and Viscoelastic Behavior of SiO_2 Films," *J. Electrochem. Soc.*, **126**, p. 1014 (1979).

9. A. Bogh and A. K. Gaind, "Influence of Film Stress and Thermal Oxidation on the Generation of Dislocations in Silicon," *Appl. Phys. Lett.*, **33**, p. 895 (1978).

10. I. Magdo and A. Bogh, "Framed Recessed Oxide Scheme for Dislocation-Free Planar Si Structures," *J. Electrochem. Soc.*, **125**, p. 932 (1978).

11. K. Shinada, S. Shinozaki, K. Kurosawa, and K. Taniguchi, "Nature and Mechanism of Emitter-Collector Short in Oxide Isolated Bipolar Integrated Circuits," *IEDM Tech. Digest*, p. 344 (1979).

12. S. M. Hu, "Formation of Stacking Faults and Enhanced Diffusion in the Oxidation of Silicon," *J. Appl. Phys.*, **45** (4), p. 1567 (1974).

13. J. Katcki, R. Gleichmann, J. Lysko, and H. Bartch, "On the Influence of Point Defects in the LOCOS Process," *Phys. Status Solidi (a)*, **101**, p. 381 (1987).

14. J. Vanhellemont and C. Claeys, "A Quantitative Model for Silicon Yield Stress at Thin Film Edges," *J. Electrochem. Soc.*, **135**, p. 1509 (1988).

15. S. M. Hu and R. O. Schwenker, "Effects of Ion-Implantation on Substrate Hardening and Film Stress Reduction and Their Effect on the Yield of Bipolar Transistors," *J. Appl. Pys.*, **49**, p. 3259 (1978).

16. S. M. Hu, S. P. Kelpner, R. O. Schwenker, and D. K. Seto, "Dislocation Propagation and Emitter Edge Defects in Silicon Wafers," *J. Appl. Phys.*, **47**, p. 4098 (1976).

17. S. M. Hu, "Stress Related Problems in Silicon Technology," *J. Appl. Phys.*, **70** (6), p. R53 (1991).

18. S. M. Hu, "Effects of Surface Films and Film Edges on Dislocation Movement in Silicon," *J. Appl. Phys.*, **46**, p. 1465 (1975).

19. C. Claeys, J. Vanhellemont, G. Declerk, J. Van Landuyt, R. Van Overstraeten, and S. Amelinckx, "Defect Control in Si_3N_4/SiO_2 Structure of Recessed SiO_2," in *VLSI Science and Technology*, Edited by K. E. Bean and G. A. Razgonyi (Electrochemical Society, Pennington, NJ, 1984), p. 272.

20. J. Vanhellemont, S. Amelinckx, and C. Claeys, "Defect Control in Si_3N_4/SiO_2 Structures for Isolation Techniques," *J. Appl. Phys.*, **61**, p. 2170 (1987).

21. P. M. Fahey, S. R. Mader, S. R. Stiffler, R. L. Mohler, J. D. Mis, and J. A. Slinkman, "Stress-Induced Dislocations in Silicon Integrated Circuits," *IBM J. of Res. and Dev.*, **36**, No. 2, p. 158 (1992).

22. Scott R. Stiffler, Jerry B. Lasky, Charles W. Koburger, and Wayne S. Berry, "Oxidation-Induced Defect Generation in Advanced DRAM Structures," *IEEE Trans. Elec. Dev.*, **37** (5), p. 1253 (1990).

23. Scott R. Stiffler and Arturo O. Cifuentes, "The Effect of Trench Corner Shapes on Local Stress Fields: A Three-Dimensional Finite-Element Modeling Study," *IEEE Trans. Elec. Dev.*, **40** (3), p. 557 (1993).

24. D. Chidambarrao, J. P. Peng, and G. R. Srinivasan, "Stresses in Silicon Substrates Near Isolation Trenches," *J. Appl. Phys.*, **70** (9), p. 4816 (1991).

25. S. M. Hu, "Stress from Isolation Trenches in Silicon Substrates," *J. Appl. Phys.*, **67**, p. 1092 (1990).

26. Wen Lin, D. W. Hill, C. L. Paulnack, M. J. Kelly, and K. E. Benson, "Misfit Stress and Dislocations in P/P+ Epitaxial Silicon Wafers: Effects and Elimination," *Proc. of the Second Symposium on Defects in Silicon*, Edited by W. Murray Bullis, Ulrich Gösele, and Fumio Shimura (The Electrochemical Society, Pennington, NJ, 1991), p. 163.

27. K.S. Jones, S. Prussin, and E.R. Weber, "A Systematic Analysis of Defects in Ion Implanted Silicon," *Appl. Phys. A.*, **45** (1), p. 1 (1988).

28. F. M. Ross, R. Hull, D. Bahnck, J. C. Bean, L. J. Peticolas, and C. A. King, "Changes in Electrical Device Characteristics During In-Situ Formation of Dislocations." *Appl. Phys. Lett.*, **62 (12)**, p. 1426 (1993).

29. Heemyong Park, K. S. Jones, and M. E. Law, "Point Defect Based Two-dimensional Model of the Evolution of Dislocation Loops in Silicon During Oxidation," *J. Electochem. Soc.*, **141**, p. 759 (1994).

30. R. B. Fair, J.J. Wortman, and J. Liu, "Modeling Rapid Thermal Diffusion of Arsenic and Boron in Silicon," *J. Electochem. Soc*, **131**, p. 2387 (1984).

31. S. D. Gavazza and D.M. Barnett, "The Self-Force on a Planar Dislocation Loop in an Anisotropic Linear-Elastic Medium," *J. Mech. Phys. Solids*, **24**, p. 171 (1976).

32. R. Bullough, J.T. Stanley, and J.M. Williams, "The Kinetics of Migration of Impurities to Small Dislocation Loops," *Met. Sci. J.*, **2**, p. 93, (1968).

33. J. Bastecka and F. Kroupa, "Elastic Interaction of Dislocation Loops and Point Defects," *Czech. J. Phys.*, **B14**, p. 443, (1964).

34. L. Borucki, "Modeling the Growth and Annealing of Dislocation Loops," Workshop on Numerical Modeling of Processes and Devices for Integrated Circuits, *NUPAD IV*, Seattle, WA (1992).

35. Jinning Liu, "A Study of Loop Evolution During Inert Ambient Annealing and Reaction Between Point Defects and Dislocation Loops During Oxidation of Silicon," Master's Thesis, Dept. of Materials Science and Engineering, University of Florida, Gainesville (1994).

36. B. L. Eyre and D. M. Maher, "Neutron Irradiation Damage in Molybdenum Part V. Mechanisms of Vacancy and Interstitial Loop Growth during Post-Irradiation Annealing," *Phil. Mag.*, p. 767 (1971).

37. J. P. Hirth and J. Lothe, *Theory of Dislocations*, 2nd ed. (John Wiley & Sons, Inc., New York, 1982), p. 497.

38. Heemyong Park, "Point-Defect-Based Two-Dimensional Modeling of Dislocation Loops and Stress Effects on Dopant Diffusion in Silicon," Doctoral Dissertation, Dept. of Electrical Engineering, University of Florida, Gainesville (1993).

39. J. D. Mis, S.R. Mader, and D.N. Beshers, "Effect of a Stress Field on Boron Implantation Damage in Silicon," *J. Appl. Phys.*, **74**, p. 2294 (1993).

40. Y. Kim, Hisham Z. Massoud, Richard B. Fair, "The Effect of Ion-Implantation Damage on Dopant Diffusion in Silicon During Shallow Junction Formation," *J. Elec. Matls.*, **18**, p. 143 (1989).

41. Robert H. Thompson Jr., "Type II Dislocation Loops and Their Effect on Strain in Ion Implanted Silicon as Studied by High Resolution X-Ray Diffraction," Master's Thesis, Dept. of Materials Science and Engineering, University of Florida, Gainesville (1994).

42. P. Zaumseil, U. Winter, F. Cembali, M. Servidori and Z. Sourek, "Determination of Dislocation Loop Size and Density in Ion Implanted and Annealed Silicon by Simulation of Triple Crystal X-Ray Rocking Curves," *Phys. Stat. Sol.*, **100a**, p. 95 (1987).

43. M. Servidori, S. Solmi, P. Zaumseil, U. Winter and M. Anderle, "Interaction Between Point Defects and Dislocation Loops as the Phenomenon able to Reduce Anomalous Diffusion of Phosphorus in Silicon," *J. Appl. Phys.*, **65**, p. 98 (1989).

44. O. C. Zienkiewicz, and R. L. Taylor, *The Finite Element Method*, Fourth Edition, Vol. 1 (McGraw-Hill Book Company, New York, 1989).

45. A. O. Cifeuntes and S. R. Stiffler, "Modeling Thermal Stresses in Periodic Structures: Some Observations Regarding Boundary Conditions," *J. Elec. Pack.*, **114**, p. 397 (1992).

46. A. O. Cifuentes, "A Note on the Determination of the Thermal Stresses in Multi-Metal Beams Subjected to Temperature Variations," *J. Elec. Pack.*, **113**, p. 397 (1991).

47. Jinning Liu, K. S. Jones and Mark E. Law, "Evolution of Dislocation Loops in Silicon in an Inert Ambient (I)," *Solid-State Elec.*, **38**, p. 1305 (1995).

48. Samir Chaudhry, Jinning Liu, K. S. Jones and Mark E. Law, "Evolution of Dislocation Loops in Silicon in an Inert Ambient (II)," *Solid-State Elec.*, **38**, p. 1313 (1995).

49. K.L. Chopra, *Thin Film Phenomena*, Chapter 5 (McGraw-Hill, New York 1969).

50. S. T. Ahn, H.W. Kennel, J.D. Plummer, and W.A. Tiller, "Film Stress-Related Vacancy Supersaturation in Silicon under Low-Pressure Chemical Vapor Deposited Silicon Nitride Films," *J. Appl. Phys.*, **64** (10), p. 4914 (1988).

51. K. Osada, Y. Zaitsu, S. Matsumoto, M. Yoshida, E. Arai, and T Abe, "Effects of Stress in the Deposited Silicon Nitride Films on Boron Diffusion in Silicon," *J. Electrochem. Soc.*, **142**, p. 202 (1995).

52. S. C. Jain, A. H. Harker, A. Atkinson, and K. Pinardi, "Edge-Induced Stress and Strain in Stripe Films and Substrates: A Two-Dimensional Finite Element Calculation," *J. Appl. Phys.*, **78** (3), p. 1630 (1995).

53. W.-M. Kuschke and E. Arzt, "Investigation of the Stresses in Continuous Thin Films and Patterned Lines by X-Ray Diffraction," *Appl. Phys. Lett.*, **64** (9), p. 1097 (1994).

54. Shoichi Mizuo and Hisayuki Higuchi, "Anomalous Diffusion of B and P in Si Directly Masked with Si_3N_4," *J. Appl. Phys.*, **21** (2), p. 281 (1982).

55. P. Kuo, J. L. Hoyt, and J. F. Gibbons, "Effects of Strain on Boron Diffusion in Si and $Si_{1-x}Ge_x$," *Appl. Phys. Lett.*, **66** (5), p. 580 (1995).

56. Heemyong Park, Kevin S. Jones, Jim A. Slinkman, and Mark E. Law, "Effects of Hydrostatic Pressure on Dopant Diffusion in Silicon," *J. Appl. Phys.*, **78** (6), p. 3664 (1995).

57. Michael Lee Manda, "Stress-Assisted Diffusion in Silicon," Doctoral Dissertation, Dept. of Mechanical Engineering and Material Science, Duke University, Durham, NC (1985).

58. Technology Modeling Associates, "MEDICI User's Manual," Technology Modeling Associates, Sunnyvale, CA (1994).

59. J. M. Poate, D. J. Eaglesham, G. H. Gilmer, H.-J. Gossmann, M. Jaraiz, C. S. Rafferty, and P. A. Stolk, "Ion Implantation and Transient Enhanced Diffusion," *IEDM Tech. Dig.*, p. 77 (1995).

60. L. H. Zhang, K. S. Jones, P. H. Chi, and D. S. Simons, "Transient Enhanced Diffusion Without {311} Defects in Low Energy B^+-Implanted Silicon," *Appl. Phys. Lett.*, **67** (14), p. 2025 (1995).

61. Nicolas Cuendet, Timur Halicioglu, and William A. Tiller, "The Energetics of {113} Stacking Fault Formation in Si from Supersaturated Interstitials," *Appl. Phys. Lett.*, **68** (1), p. 19 (1996).

62. M. E. Law and K. S. Jones, "{311} Defect Formation and Evolution for Si and B Implants," *Proc. of the Fourth International Symposium on Process Physics and Modeling of Semiconductor Devices*, (Electrochemical Society, Los Angeles, 1996).

63. Hernan Rueda, Stephen Cea, Samir Chaudhry, and Mark E. Law, "Multidimensional Modeling of Stress Related Effects in Silicon Technology," Dept. of Electrical and Computer Engineering, University of Florida, Gainesville, unpublished paper, 1996..

BIOGRAPHICAL SKETCH

Samir Chaudhry was born in Meerut, India, on 27th August 1969. He received his B.E. degree in electronics and communication engineering, with a first class (distinction), from the University of Madras, India, in 1991, and his M.S. degree in electrical engineering from the University of Florida, Gainesville, Florida, in 1993. His research for his M.S. degree was on the effects of low dose carbon, oxygen, and silicon implantation damage on the diffusion of phosphorus. Since then, he has been working towards a Ph.D. degree in electrical engineering at the University of Florida. His research interests are in the field of semiconductor process modeling, simulation, and integration, with emphasis on the development of predictive stress models for use in ULSI process development and design. He is a member of Tau Beta Pi and the Electrochemical Society.

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Robert M. Fox
Associate Professor of Electrical and Computer Engineering

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Toshikazu Nishida

Toshikazu Nishida
Associate Professor of Electrical and Computer Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Kevin S. Jones
Associate Professor of Materials Science and Engineering

This dissertation was submitted to the Graduate Faculty of the College of Engineering and to the Graduate School and was accepted as partial fulfillment of the requirements for the degree of Doctor of Philosophy.

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Dean, College of Engineering

Karen A. Holbrook
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